A New Topology of Bidirectional Buck-Boost dc/dc Converter with Capability of Soft Switching and input Current Ripple Cancellation

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Abstract: In this paper, a new bidirectional buck-boost dc-dc converter with capability of soft switching and zero input current ripple is proposed. The coupled inductor is used in the proposed converter to eliminate the input current ripple. In the proposed converter, zero voltage switching (ZVS) and zero current switching (ZCS) can be obtained for the main and auxiliary switches, respectively. In addition, the proposed topology is analyzed in all operating modes and all equations of voltage and current for components are obtained. Moreover, the required conditions for soft switching operation and also achieving zero input current ripple are calculated. Finally, the acuracy performance of the proposed converter is reconfirmed through simulation results in EMTDC/PSCAD software program.

Keywords: Bidirectional dc-dc Converter; Active Snubber; Zero Voltage Switching; Zero Input Current Ripple.

1 Introduction

Nowadays, the bidirectional dc-dc converters with capability of soft switching have received more attentions because of low losses. Moreover, the converters that are able to eliminate the input current ripple have most importance. In [1-4], several high power full-bridge isolated dc-dc converters with the capability of soft switching have been presented. In these converters, the input current value is equal to the switches current value for the high value of duty cycle. In addition, the high value of input current ripple is made by turning on and off the switches. In [5], a buck-boost bidirectional dc-dc converter based on coupled inductor has been presented. In this converter, the soft switching is obtained by using the resonance condition between coupled inductor and capacitors. The resonance frequency must be less than the switching frequency. Moreover, the converter has considerable ripple in input current. A new three-phase bidirectional dc-dc converter has been presented in [6]. The drawback of this converter is high input current ripple. In [7-9], several methods to eliminate the output voltage ripple in the buck and buck-boost dc-dc converters have been presented. In these topologies, in order to eliminate the output voltage ripple, the minimum values of inductor and capacitor have been calculated. In these topologies, due to hard switching its losses are inevitable. The isolated bidirectional dc-dc converters have higher voltage losses and lower efficiency in comparison with the nonisolated bidirectional dc-dc converters [10-12]. In [13], a dc-dc converter based on coupled inductors with three windings and high voltage gain has been presented. In this topology, the coupled inductors are used to generate high voltage gain and used switches are operating at ZCS. In addition, this topology has low voltage stress in high power applications. In [14], a bidirectional dc-dc converter with capability of soft switching has been presented. This topology is able to provide ZVS for all switches by using auxiliary circuit. This circuit includes of additional inductor and capacitor. In addition, high value of circulating current without considering the value of the load is crossed from auxiliary inductor and capacitor. This is the main problem of this topology that leads to high conductive losses of converter. In [15], a bidirectional dc-dc converter with the capability of soft switching and zero input current ripples has been presented. The problem of this converter is its high inductive losses due to high circulating current in all operating modes of the converter. In [16], a bidirectional four-phase dc-dc converter has been presented. In this topology, elimination the input current ripple of the conventional bidirectional dc-dc converter is considered. High

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number of used switching elements and inductors in input side are disadvantages of this converter. In order to overcome the high inductive losses and circulating current in the bidirectional dc-dc converters with soft switching, the dc-dc converter with soft switching technique has been presented in [17]. In this topology, the crossed current from the auxiliary circuit is extremely decreased in comparison with the conventional converters because of operating the active snubber in the short time intervals. As a result, the inductive losses in the main switches and auxiliary circuits are extremely decreased and the efficiency of the converter is increased. In [18] a bidirectional dc-dc converter has been presented. This converter uses the coupled inductor for achieving zero voltage switching. It has the input current ripple for all the time during a switching period.

In this paper, a new bidirectional buck-boost dc-dc converter to eliminate input current ripple in all ranges of duty cycles is proposed. The proposed converter is completely analyzed in different operating modes in buck and boost operations. In addition, the voltage gain, the current and voltage equations of all elements are calculated. Finally, the accuracy performance of the proposed converter is reconfirmed through simulation results in EMTDC/PSCAD software program.

2 Proposed Converter

The power circuit of the proposed bidirectional converter is shown in Fig. 1. This topology can operate as the buck and boost dc-dc converter. The diodes of D_1, D_2, D_3 and D_4 are the internal diodes of the switches S_1, S_2, S_3 and S_4. The capacitors of C_1 and C_2 are the parasitic capacitors of the switches S_1 and S_2, respectively. The lossless active snubber consists of an auxiliary inductor L_2, a capacitor C_4, clamper diodes of D_5 and D_6, and the auxiliary switches of S_3 and S_4. The voltage of capacitor C_4 is considered as a voltage source V_{C4} in the time interval of switching if high value of the capacitance is considered. In order to decrease the circulating current of the lossless active snubber and providing the soft switching conditions for the switches of S_1 and S_2, the active snubber will be in the circuit for the short time interval. The diodes of D_7 and D_8 act as the clamping voltage in the auxiliary switches of S_3, S_4 and the clamper diodes of D_5 and D_6 from the snubber circuit. In order to turning on the switch S_1 in ZVS state for the boost operating mode, firstly, the internal diode is turned on and after short time interval of applying trigger pulse to it, by changing the current direction of the diode this switch is turned on. The same condition is valid for S_2 in buck operating mode. In this mode, the internal diode of the switch S_1 is conducted for a long time interval and the ZVS is usually made in this switch. The same condition is valid for S_2 in the boost operating mode. The coupled inductors with the inductance of L_P for the primary winding, L_S for the secondary winding and M for the coupling inductance are used to eliminate the input current ripple. The voltage of V_{C3} is equal to the voltage source V_ℓ in the time interval of switching if the value of the capacitance is considered high enough. As a result, the inductors of L_P and L_S are connected in parallel and their voltage are same, so, their equivalent inductance is lower than the voltage of L_P and L_S separately.

2.1 Boost Operating State

The voltage and current waveforms of the proposed converter in boost operating mode are shown in Fig. 2. The equivalent circuits of the proposed converter by replacing the transformer model of the coupled inductors are shown in Fig. 3. The coupling factor, the value of inductances L_k and L_m are defined as follows:

$$K = \frac{M}{\sqrt{L_P L_S}} \tag{1}$$

$$L_k = (1-K^2)L_P \tag{2}$$

$$L_m = K^2 L_P \tag{3}$$

As the transformers ratio (n) is equal to the division of the number of the primary winding N_P to the number of the secondary winding N_S, the effective ratio N_e is calculated as follows:

$$N_e = \sqrt{\frac{L_S}{L_P}} = nK \tag{4}$$

First Operating Mode ($t_0 \le t < t_1$):

The equivalent circuit of the first operating mode is shown in Fig. 3(a). In this operation, the parasitic capacitor C_2 is charged and the parasitic capacitor C_1 is discharged. As the time interval of this operation is very low, it is possible to consider the current values of the inductances i_{L2}, i_{Lm} and i_{Lk} equal to their minimum values $-I_{s2}$, I_{m2} and I_{k2}, respectively. According to the fact that the voltage of capacitor C_1 has to be discharged completely to the zero value in this operating mode, the diode of D_1 is turned on. The time interval of the first operating mode (T_1) is calculated as follows:

$$T_1 = \frac{n(C_1 + C_2)V_H}{nI_{s2} - (n-1)I_{k2} - I_{m2}} \tag{5}$$

Second Operating Mode ($t_1 \le t < t_2$):

The equivalent circuit of this mode is shown in Fig. 3(b). The switch of S_1 is turned on in the ZVS state. Based on the equivalent circuit, the voltage of the

inductors L_m, L_k and L_2 are equal to V_ℓ / n, $v_{Lp} - v_{Lm}$ and V_{C4}, respectively. The current of these inductors are linearly increased. So according to the auxiliary circuit in the input section we have $v_{Lp} = v_{Ls} = nv_{Lm} = V_\ell$. Therefore it can be written:

$$i_{Lm} = \frac{V_\ell}{nL_m}(t - t_1) + I_{m2} \tag{6}$$

$$i_{Lk} = \frac{(n-1)V_\ell}{nL_k}(t - t_1) + I_{k2} \tag{7}$$

$$i_{PS} = i_{Lk}\left(1 - \frac{1}{n}\right) + \frac{i_{Lm}}{n} = \left[\left(\frac{n-1}{n}\right)^2 \frac{V_\ell}{L_k} + \frac{V_\ell}{n^2 L_m}\right](t - t_5) + \left(\frac{n-1}{n}\right) I_{k2} + \frac{I_{m2}}{n} \tag{8}$$

$$i_{L2} = -I_{s2} + \frac{V_{C4}}{L_2}(t - t_1) \tag{9}$$

The current i_{S1} is equal to sum of the current of the inductors i_{PS} and i_{L2} based on Eqs. (8) and (9).

Third Operating Mode ($t_2 \le t < t_3$):

The equivalent circuit of the proposed converter in this operating mode is shown in Fig. 3(c). When the current of i_{L2} and so the voltage of v_{L2} are equal to zero, the switch of S_4 is turned off in ZCS state. The current of the switch S_1 is equal to the current of i_{PS} from (8).

Fourth Operating Mode ($t_3 \le t < t_4$):

The equivalent circuit of the proposed converter in this operating mode is shown in Fig. 3(d). As the voltage v_{L2} is equal to V_{C4}, therefore it can be written:

$$i_{L2} = \frac{V_{C4}}{L_2}(t - t_3) \tag{10}$$

The current of i_{s1} is equal to sum of the current of i_{PS} from Eq. (8) and the current of i_{L2} from Eq. (10).

By considering Eqs. (6), (7) and (10) and Fig. 2, it is obtained that:

$$I_{m1} = I_{m2} + \frac{V_\ell}{nL_m} DT_s \tag{11}$$

$$I_{k1} = I_{k2} + \frac{(n-1)V_\ell}{nL_k} DT_s \tag{12}$$

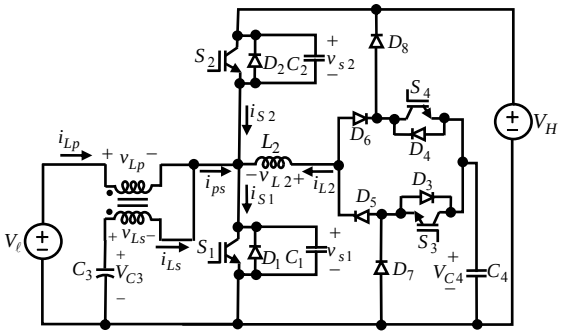

Fig. 1 The proposed bidirectional dc-dc converter with soft switching.

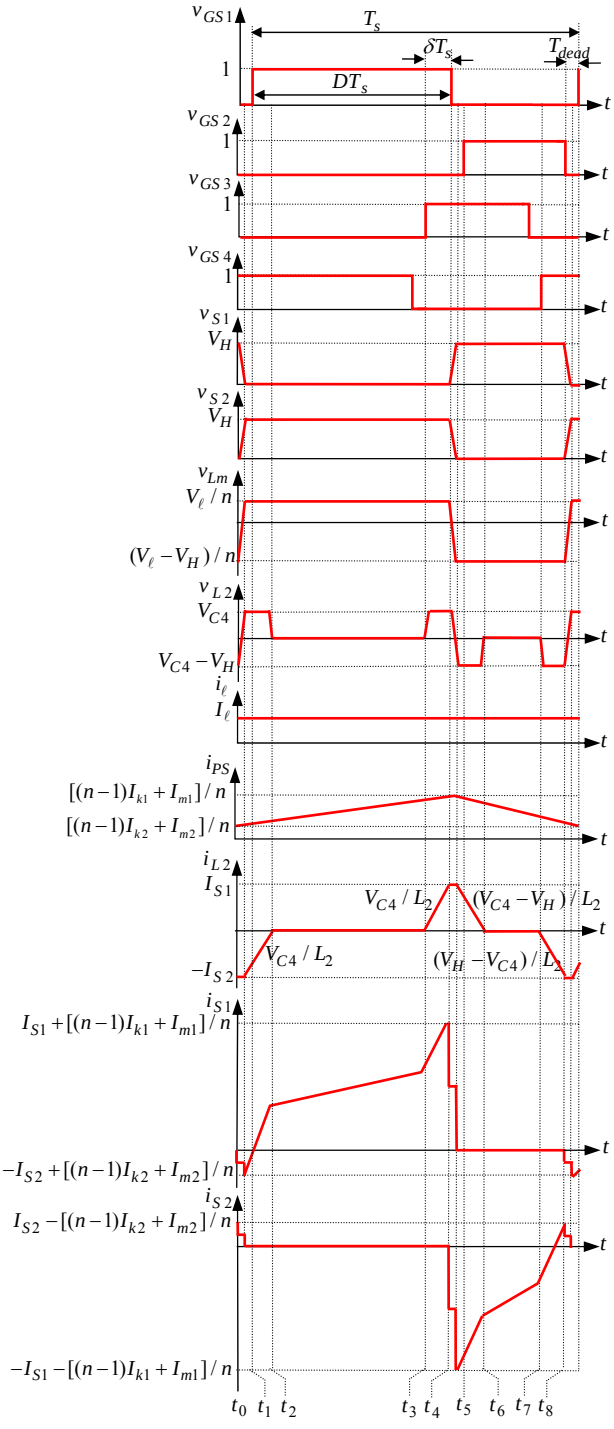

Fig. 2 The waveforms of the proposed converter in the boost operation.

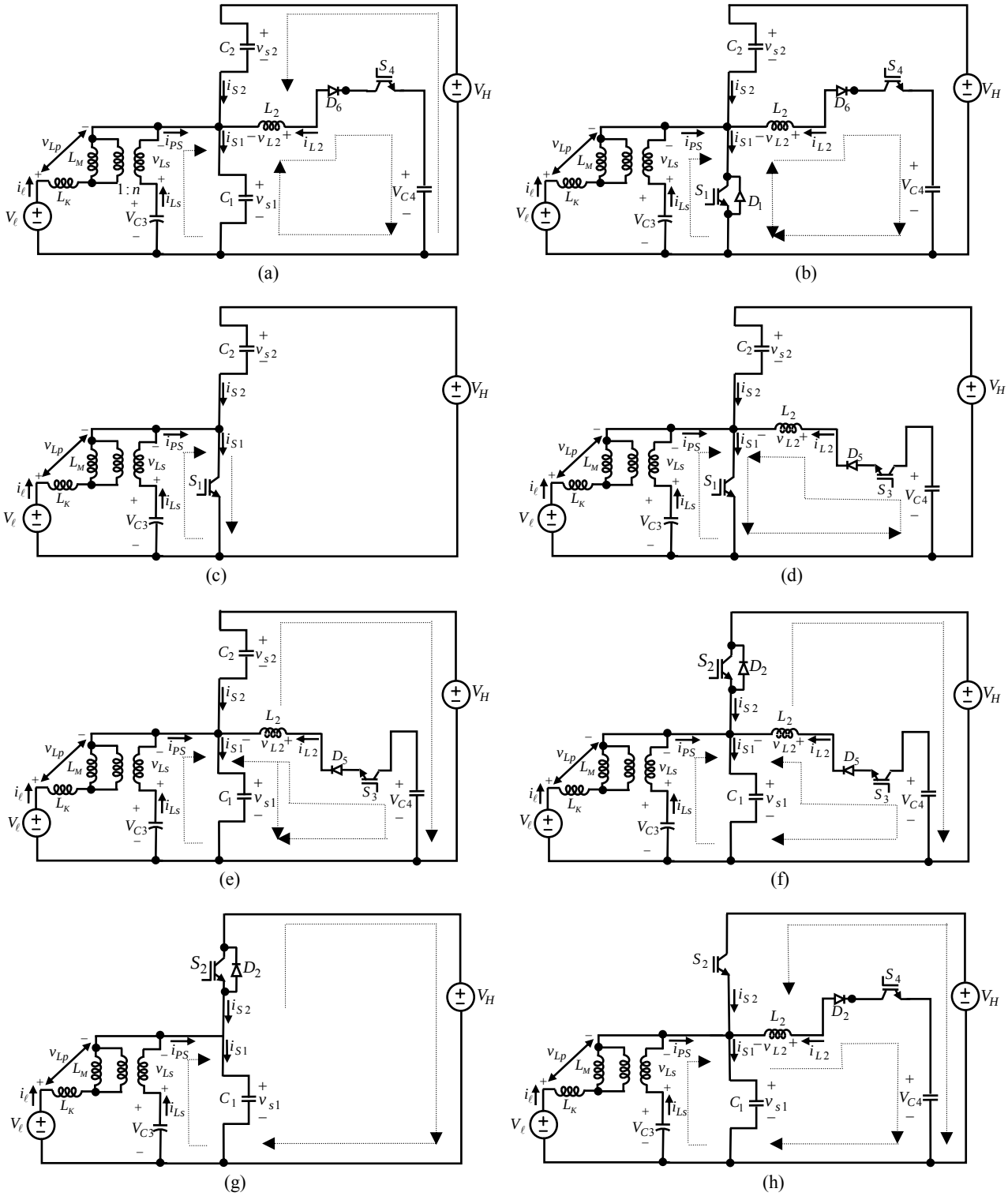

Fig. 3 The equivalent circuits of the proposed converter in boost operation.

$$I_{s1} = \frac{V_{C4}}{L_2}\delta T_s \tag{13}$$

where D is the duty cycle and δT_s is the time interval that the auxiliary inductance of L_2 is charged.

Fifth Operating Mode ($t_3 \le t < t_4$):

The equivalent circuit of this operating mode is shown in Fig. 3(e). The capacitor C_1 is charged and the capacitor C_2 is discharged. As the time interval of this operating mode is very short, it is possible to consider the current value of the inductors i_{Lm}, i_{Lk} and i_{L2} equal

to their maximum values as I_{s1}, I_{m1} and I_{k1}, respectively. Similar to first mode, the time interval of the fifth operating mode T_2 is calculated as follows:

$$T_2 = \frac{n(C_1 + C_2)V_H}{nI_{s1} + I_{m1} + (n-1)I_{k1}} \tag{14}$$

Sixth Operating Mode ($t_5 \le t < t_6$):

The equivalent circuit of this operating mode is shown in Fig. 3(f). The switch S_2 turn on at ZVS state. The voltage of the inductors L_m, L_k and L_2 are equal to $(V_\ell - V_H)/n$, $v_{Lp} - v_{Lm}$ and $V_{C4} - V_H$, respectively. Based on auxiliary circuit at the input section of the converter, it is resulted that $v_{Lp} = v_{Ls} = nv_{Lm} = V_\ell - V_H$. Therefore, it can be written:

$$i_{Lm} = \frac{(V_\ell - V_H)}{nL_m}(t - t_5) + I_{m1} \tag{15}$$

$$i_{Lk} = \frac{(n-1)(V_\ell - V_H)}{nL_k}(t - t_5) + I_{k1} \tag{16}$$

$$\begin{aligned} i_{PS} &= i_{Lk}\left(1 - \frac{1}{n}\right) + \frac{i_{Lm}}{n} \\ &= \left[\left(\frac{n-1}{n}\right)^2 \frac{(V_\ell - V_H)}{L_k} + \frac{(V_\ell - V_H)}{n^2 L_m}\right](t - t_5) \\ &\quad + \left(\frac{n-1}{n}\right)I_{k1} + \frac{I_{m1}}{n} \end{aligned} \tag{17}$$

$$i_{L2} = I_{s1} + \frac{(V_{C4} - V_H)}{L_2}(t - t_5) \tag{18}$$

The current i_{S2} is equal to sum of the current $-i_{PS}$ from Eq. (17) and current $-i_{L2}$ from Eq. (18).

Seventh Operating Mode ($t_6 \le t < t_7$):

The equivalent circuit of this operating mode is shown in Fig. 3(g). This operating mode is started when the current of i_{L2} and the voltage of v_{L2} are equal to zero. The switch of S_3 is turned off in ZCS state. The current of the switch S_2 is equal to current $-i_{PS}$ from Eq. (17).

Eighth Operating Mode ($t_7 \le t < t_8$):

The equivalent circuit of this operating mode is shown in Fig. 3(h). As the voltage value of L_2 is equal to $V_{C4} - V_H$ so, it is resulted that:

$$i_{L2} = \frac{V_{C4} - V_H}{L_2}(t - t_7) \tag{19}$$

The current i_{s2} is equal to sum of the current $-i_{L2}$ from Eq. (19) and current $-i_{PS}$ from Eq. (17). According to Fig. 2 and by considering Eqs. (15), (16) and (19), it is resulted that:

$$I_{m2} = I_{m1} + \frac{V_\ell - V_H}{nL_m}(1 - D)T_s \tag{20}$$

$$I_{k2} = I_{k1} + \frac{(n-1)(V_\ell - V_H)}{nL_k}(1 - D)T_s \tag{21}$$

$$-I_{s2} = \frac{V_{C4} - V_H}{L_2}\delta T_s \tag{22}$$

2.2 Buck Operating State

The voltage and current waveforms of the proposed topology in buck operating mode are shown in Fig. 4. By comparing Figs. 2 and 4, it is clear that the converter's waveforms in the buck and boost operating modes are same and only the currents' direction of L_m, L_k, S_1 and S_2 are changed. The equivalent circuits of the converter in buck operating mode are as same as the boost operating mode. Table 1 summarizes the equations of the converter for buck operation.

Table 1 Summarized results for buck operation.

Operating Modes	Equations
1th Mode ($t_0 \le t < t_1$)	$T_1 = \frac{n(C_1 + C_2)V_H}{I_{m1} + nI_{s2} + (n-1)I_{k1}}$
2th Mode ($t_1 \le t < t_2$)	$i_{Lm} = -I_{m1} + \frac{V_\ell}{nL_m}(t - t_1)$ $i_{Lk} = -I_{k1} + \frac{(n-1)V_\ell}{nL_k}(t - t_1)$ $i_{PS} = \left[\left(\frac{n-1}{n}\right)^2 \frac{V_\ell}{L_k} + \frac{V_\ell}{n^2 L_m}\right](t - t_5) - \left(\frac{n-1}{n}\right)I_{k1} - \frac{I_{m1}}{n}$
3th Mode ($t_2 \le t < t_3$)	$i_{S1} = \left[\left(\frac{n-1}{n}\right)^2 \frac{V_\ell}{L_k} + \frac{V_\ell}{n^2 L_m}\right](t - t_5) - \left(\frac{n-1}{n}\right)I_{k1} - \frac{I_{m1}}{n}$
4th Mode ($t_3 \le t < t_4$)	$-I_{m2} = -I_{m1} + \frac{V_\ell}{nL_m}DT_s$ $-I_{k2} = -I_{k1} + \frac{(n-1)V_l}{nL_k}DT_s$
5th Mode ($t_4 \le t < t_5$)	$T_2 = \frac{n(C_1 + C_2)V_H}{nI_{s1} - I_{m2} - (n-1)I_{k2}}$
6th Mode ($t_5 \le t < t_6$)	$i_{Lm} = -I_{m2} - \frac{V_H - V_\ell}{nL_m}(t - t_5)$ $i_{Lk} = -I_{k2} + \frac{(n-1)(V_l - V_H)}{nL_k}(t - t_5)$ $i_{PS} = \left[\left(\frac{n-1}{n}\right)^2 \frac{(V_\ell - V_H)}{L_k} + \frac{V_\ell - V_H}{n^2 L_m}\right](t - t_5)$ $-\left(\frac{n-1}{n}\right)I_{k2} - \frac{I_{m2}}{n}$
7th Mode ($t_6 \le t < t_7$)	$i_{S2} = -i_{PS} = \left(\frac{n-1}{n}\right)I_{k2} + \frac{I_{m2}}{n}$ $-\left[\left(\frac{n-1}{n}\right)^2 \frac{(V_\ell - V_H)}{L_k} + \frac{V_\ell - V_H}{n^2 L_m}\right](t - t_5)$
8th Mode ($t_7 \le t < t_8$)	$-I_{m1} = -I_{m2} - \frac{V_H - V_\ell}{nL_m}(1 - D)T_s$ $-I_{k1} = -I_{k2} + \frac{(n-1)(V_\ell - V_H)}{nL_k}(1 - D)T_s$

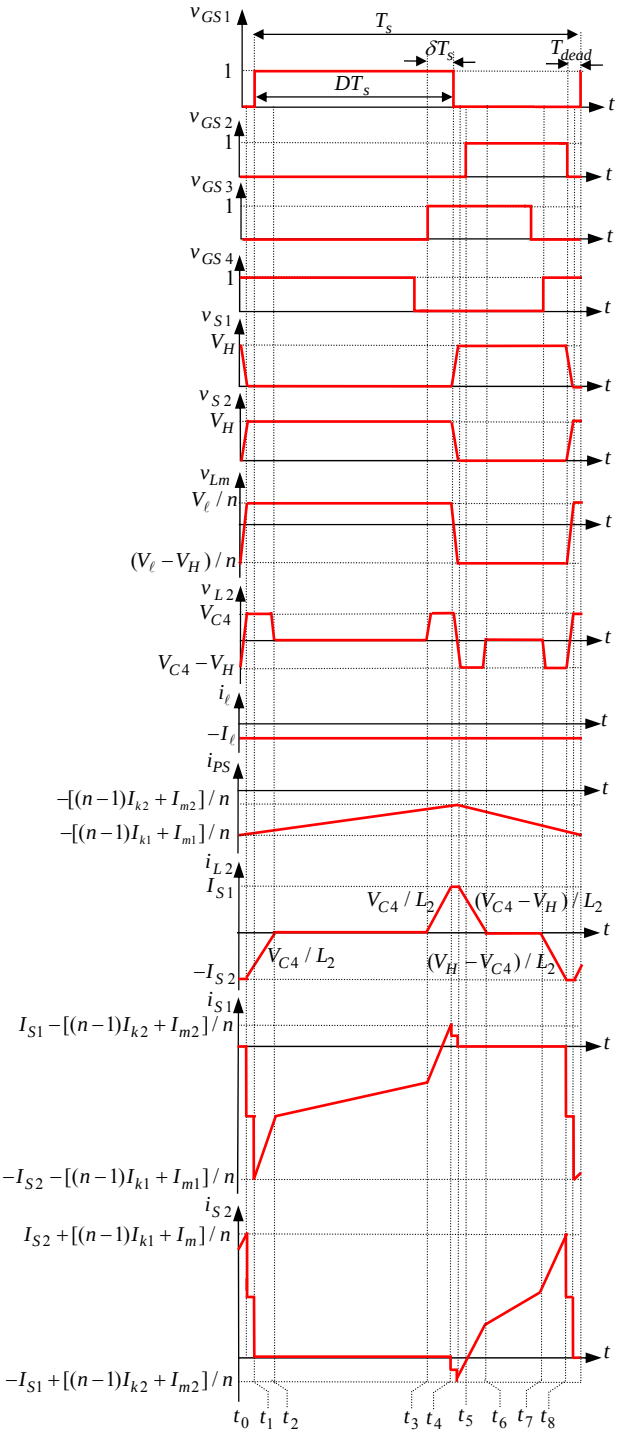

Fig. 4 Waveforms for Buck operation.

3 Auxiliary Capacitor Voltage Calculation

By applying the voltage balance law for L_2, the following equation is obtained:

$$(\delta T_s + \delta_{12} T_s) V_{C4} = (\delta T_s + \delta_{56} T_s)(V_H - V_{C4}) \quad (23)$$

where $\delta_{12} T_s$ and $\delta_{56} T_s$ are the time intervals between t_1 to t_2 and t_5 to t_6, respectively. By considering the current balance law for C_4, we have:

$$\frac{1}{2}(\delta T_s + \delta_{12} T_s) I_{s2} = \frac{1}{2}(\delta T_s + \delta_{56} T_s) I_{s1} \quad (24)$$

Based on Eqs. (23) and (24), the voltage of the capacitor C_4 for the buck and boost operating modes is obtained as follows:

$$V_{C4} = \frac{V_H}{2} \quad (25)$$

By replacing Eq. (25) into Eqs. (13) and (22), the current values of I_{s1} and I_{s2} are obtained by:

$$I_{s1} = I_{s2} = \frac{V_H}{2L_2} \delta T_s \quad (26)$$

The current of i_{L2} is independent to the load value, therefore, the voltage of V_{C4} is also independent to the load value.

4 Main Inductor Current Calculation

By applying KCL in Fig. 2, it is resulted that:

$$i_{Lk} - i_{Lm} = -n i_{Ls} \quad (27)$$

As the average current value of the capacitor C_1 is equal to zero and by considering Fig. 1, the value of current i_{Ls} is equal to $-i_{C1}$. So, it is resulted that the average values of i_{Lk} and i_{Lm} are equal to I_ℓ. Therefore based on Fig. 2, it can be written:

$$I_\ell = \frac{(I_{m1} + I_{m2})}{2} = \frac{I_{k1} + I_{k2}}{2} \quad (28)$$

By replacing the value of current I_{m2} from Eq. (28) into Eq. (11) we have Eqs. (29)-(30). By replacing the value of current I_{k2} from Eq. (28) into Eq. (21) we have Eqs. (31)-(32).

$$I_{m1} = I_\ell + \frac{V_\ell}{2nL_m} DT_s \quad (29)$$

$$I_{m2} = I_\ell - \frac{V_\ell}{2nL_m} DT_s \quad (30)$$

$$I_{k2} = I_\ell - \frac{(n-1)V_\ell}{2nL_k} DT_s \quad (31)$$

$$I_{k1} = I_\ell + \frac{(n-1)V_\ell}{2nL_k} DT_s \quad (32)$$

According to above equations, the input current ripple is equal to:

$$\Delta i_{Lk} = I_{k1} - I_{k2} = \frac{(n-1)V_\ell}{nL_k} DT_s \quad (33)$$

5 Input Current Ripple Elimination

It is pointed out that it is impossible to calculate the input current ripple elimination because the time intervals of the first and fifth operating modes are very short. for second, third and fourth operating modes, the voltage values of the primary and secondary windings of the coupled inductors are equal to V_ℓ. As a result it is obtained that:

$$L_P \frac{di_{Lp}}{dt} + M \frac{di_{Ls}}{dt} = M \frac{di_{Lp}}{dt} + L_S \frac{di_{Ls}}{dt} = V_\ell \quad (34)$$

By simplifying (34), it is resulted that:

$$\frac{di_{LP}}{dt} = \frac{L_S - M}{L_S L_P - M^2} V_\ell \quad (35)$$

According to Eq. (35), the required conditions for zero input current ripple is obtained as follows:

$$L_s = M = K\sqrt{L_P L_S} \quad or \quad K = \sqrt{\frac{L_S}{L_P}} \quad (36)$$

$$M \neq \sqrt{L_p L_s} \quad or \quad K \neq 1 \quad (37)$$

In sixth, seven and eight operating modes, the voltage of the primary and secondary windings of the transformers are equal to $V_\ell - V_H$. The required conditions to eliminate input current ripple for all operating modes based on Eqs. (36) and (37) are obtained. As a result, Eqs. (36) and (37) are used to provide zero input current ripple. By considering $N_e = K$ and or based on Eq. (4), by assuming the transformer ratio value as $n = 1$ in the equivalent circuit of Fig. 3, the input current ripple is equal to zero. In addition, Eq. (33) reconfirms that the zero input current ripple is obtained if $n = 1$ and Eq. (37) is considered.

6 Voltage Gain Calculation

The average value of the inductor L_P is equal to the zero based on the balance law in steady state. As a result, the value of voltage gain is calculated as follows:

$$\frac{V_H}{V_\ell} = \frac{1}{1-D} \quad (38)$$

7 ZVS Condition For Main Switches

After the end of first operating mode, firstly the diode D_1 is turned on and then the switch S_1 is turned on. Therefore, at the beginning of the second operating mode the current of diode D_1 is positive and the current i_{s1} is negative. As shown in Fig. 2 and based on the current values at the time of t_1, the required conditions for the ZVS is obtained as follows:

$$i_{PS}\Big|_{t=t_0} - I_{s2} < 0 \quad (39)$$

$$T_{dead} < T_{Ds1} \quad (40)$$

where T_{dead} is the dead time for the switches S_1 and S_2 to operate in the ZVS state. T_{Ds1} is the reverse bias time of switch S_1. In this time interval, by decreasing the voltage value of the switch S_1 to zero, the reverse current is passed from D_1. By considering the time of T_{dead} and before the current direction of the inside diodes of the switches S_1 and S_2 are changed, the required pulses have to be applied to these switches. In addition, the time interval between t_0 and t_1 has to be eliminated because this time interval is very short in comparison with the times of T_{dead} and T_{Ds1}. The value of current i_{S1} in the second operating mode is equal to the sum of i_{PS} and i_{L2} from (8) and (9), respectively. As a result, in this operating mode, the minimum value of i_{S1} based on Fig. 2 is calculated as follows:

$$\left[\left(\frac{n-1}{n}\right)^2 \frac{V_\ell}{L_k} - \frac{V_\ell}{n^2 L_m} + \frac{V_{C4}}{L_2}\right] T_{Ds1} = I_{s2} - \left(\frac{n-1}{n}\right) I_{k1} - \frac{I_{m2}}{n} \quad (41)$$

By considering $T_{dead} = T_s/100$ in the boost operation state, the ZVS condition for the switch S_1 is obtained as follows:

$$\delta T_s > \frac{2L_2(1-D)P_o}{\eta V_\ell^2} - \frac{L_2(1-D)}{n^2}\left(D - \frac{1}{50}\right) T_s \left[\frac{(n-1)^2}{L_k} + \frac{1}{L_m}\right] + \frac{T_s}{100} \quad (42)$$

In boost performance state and at the end of fourth operating mode the switch S_1 is turned off. After the time of T_2 which is very short, the diode of D_2 is turned on and very high current is passed from it. As a result, the ZVS state is always existed for the switch S_2. Therefore, in boost operation, the ZVS for the switches of S_1 and S_2 at the high power is obtained by regulating the time of δT_s from Eq. (42).

Similarly, the ZVS state for switch S_2 in the buck operating mode is made by the following conditions:

$$i_{PS}\Big|_{t=t_0} - I_{s1} < 0 \quad (43)$$

$$T_{dead} < T_{Ds2} \quad (44)$$

where T_{Ds2} is the time that the main switch of S_2 is in reverse bias state and its current is passed from diode D_2. It is possible to eliminate the time interval between t_4 and t_5 because this time is very short in comparison with the times of T_{dead} and T_{Ds1}. The current of i_{S2} in the sixth operating mode is equal to sum of the currents i_{s2} and i_{L2} from Eqs. (17) and (18). As a result, the minimum value of the current i_{S2} in the sixth operating mode based on Fig. 5 is calculated as follows:

$$\left[\left(\frac{n-1}{n}\right)^2 \frac{V_\ell - V_H}{L_k} - \frac{V_\ell - V_H}{n^2 L_m} + \frac{V_{C4} - V_H}{L_2}\right] T_{Ds2} = -I_{s1} + \left(\frac{n-1}{n}\right) I_{k2} + \frac{I_{m2}}{n} \quad (45)$$

By considering $T_{dead} = T_s/100$ in the buck operating state, the ZVS state for the switch S_2 is obtained as follows:

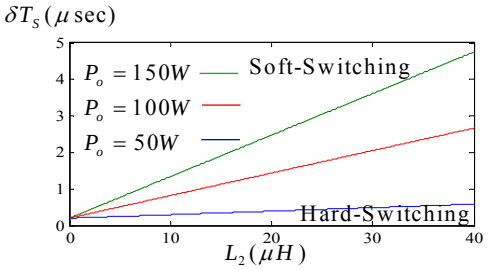

Fig. 5 The ZVS performance region versus P_H.

$$\delta T_s > \frac{2L_2(1-D)P_o}{V_l^2} - \frac{L_2}{n^2}D\left(1-D-\frac{1}{50}\right)\left(\frac{(n-1)^2}{L_k}+\frac{1}{L_m}\right)T_s+\frac{T_s}{100} \quad (46)$$

In the buck performance and at the end of the eight operating mode, the switch S_1 is turned off. After very short time of T_{t1}, the diode D_1 is turned on and very high current is passed from it. As a result, the ZVS is always made for the switch of S_1. Therefore, in the buck operation, the ZVS for the switches of S_1 and S_2 at the high power is obtained by regulating the time of δT_s from Eq. (46).

8 Comparing The Proposed Converter With The Presented Converters In [17]

In this section, in order to investigate the advantages and disadvantages of the proposed converter this topology is compared with the presented dc-dc converters in [17] and [18].

Firstly, the proposed converter is compared with the presented topology in [17]. The value of voltage gain in the proposed converter is as same as the presented converter in [17]. In both converters, the voltage stress value of the main switches is equal to V_H and the voltage stress value of the auxiliary switches is equal to $V_H/2$. As shown in Table 2, the input current ripple of the proposed topology is completely depended on the value of transformer ratio (n) and is usually decreased. The current ripple value is equal to zero by considering $n=1$. By increasing the value of n from one ($n\geq 1$), the maximum switch current stress value is decreased. Its maximum values is equal to the presented topology in [17] by considering $n=1$. In the proposed topology, the required conditions for ZVS state is as same as the presented topology in [17] while $n=1$. In addition, the required conditions to operating the ZVS in the proposed topology are depended on the value of P_ℓ and for different values of P_ℓ, the performance region is decreased and or increased. By considering $L_m = 96\,\mu\mathrm{H}$, $D=0.7$, $T_s = 20\,\mu\mathrm{sec}.$, $V_\ell = 24\,\mathrm{V}$ and $n=1$, the equation (42) is shown in Fig. 5.

As shown in this figure the performance region of ZVS state for different values of $P_\ell = 50\,\mathrm{W}, 100\,\mathrm{W}, 150\,\mathrm{W}$ is different. Moreover, in order to compensate the reduction which is made based on increasing the value of P_ℓ, the time interval of δT_s for the constant value of L_2 has to be increased and or it is possible to decrease the value of inductor L_2 for the constant value of time interval (δT_s) to obtain the ZVS performance.

In [A18] the ZVS operating conditions for the switches S_1 and S_1 are obtained by using T equivalent circuit of the coupled inductors and based on the ripple value of the inductor L_3. In other word, after the dead time between turning on and off states of two main switches (in this state the voltage of the main switch will be equal to zero because of the charging and discharging the interval capacitors of the main switches), the internal diode of the switch S_1 is conducted while its current is positive and required pulses is applied to this switches. After very short time, the switch of S_1 is turned on in the ZVS state when the diode current will be zero. In this paper, the current ripple value of the inductor L_3 based on the converter circuit parameters is obtained. It is considered that the value of the ΔI_3 has to be high when the value of $I_{L3\max}$ (that is equal to $I_{L1\max}$ for instance in the buck operating mode and for low load) is very big. As shown in the current waveforms of i_{L1}, the current of the inductor L_1 consists of ripple in all time intervals and the current ripple value r_{L1} is equal to 40% of the average load current.

In the proposed converter, by determining the parameters of the coupled inductors based on (33), (36) and (37), the required condition for zero input current ripple is obtained. It is important to note that it is possible to obtain ZVS operating state for the main switches of the proposed converter by using auxiliary circuit that consists of auxiliary switches (S_3, S_4), inductor L_2 and capacitor C_4. According to this condition, (42) and (46) show the ZVS operating state for the power switches in the boost and buck operating modes. In other word, by adjusting the time interval of δT_s from Fig. 5, the ZVS operating state is obtained. In the proposed topology as same as presented topology in [A17], the required time for charging and discharging of the parasitic capacitor has to be lower than the dead time of the main switches. In this condition, it is possible to turn on the internal diode of these switches when the positive currents are passed from them.

The voltage gain of the proposed topology and presented topology in [18] is as same as the voltage gain of the conventional buck and boost converters. In both

converters, 4 switches are required. In the presented topology of the attached paper, one the switches of S_{a1} and or S_{a2} are always turned on (the switch S_{a1} is only turned on in the buck state and the switches S_{a2} is only turned on in the boost state). These switches are lossless. In this topology, two auxiliary switches (S_3, S_4) are always turned off in the ZCS state and so their losses are only considered in turning on state of the switches.

Table 2 Comparing the proposed topology with the presented bidirectional converter in [17].

	Proposed converter	Presented topology in [17]
$\frac{V_H}{V_\ell}$	$\frac{V_H}{V_\ell}=\frac{1}{1-D}$	$\frac{V_H}{V_\ell}=\frac{1}{1-D}$
V_{C4}	$V_{C4}=\frac{V_H}{2}$	$V_{C4}=\frac{V_H}{2}$
v_{S2} , v_{S1}	$v_{S1}=v_{S2}=V_H$	$v_{S1}=v_{S2}=V_H$
I_{s1}, I_{s2}	$I_{s1}=I_{s2}=\frac{V_H}{2L_2}\delta T_s$	$I_{s1}=I_{s2}=\frac{V_H}{2L_2}\delta T_s$
I_{m1}, I_{m2}	$I_{m1}=I_\ell+\frac{V_\ell}{2L_m}DT_s$ $I_{m2}=I_\ell-\frac{V_\ell}{2L_m}DT_s$	$I_{m1}=I_\ell+\frac{V_\ell}{2nL_m}DT_s$ $I_{m2}=I_\ell-\frac{V_\ell}{2nL_m}DT_s$
δT_s	$\delta T_s\|_{BOOST}>\frac{2L_2(1-D)P_\ell}{V_\ell^2}-\frac{L_2(1-D)}{L_m}\left(D-\frac{1}{50}\right)T_s+\frac{T_s}{100}$ $\delta T_s\|_{BUCK}>\frac{2L_2(1-D)P_\ell}{V_\ell^2}-\frac{L_2}{L_m}D\left(1-D-\frac{1}{50}\right)T_s+\frac{T_s}{100}$	$\delta T_s\|_{BOOST}>\frac{2L_2(1-D)P_o}{\eta V_\ell^2}-\frac{L_2(1-D)}{n^2}\left(D-\frac{1}{50}\right)T_s\left[\frac{(n-1)^2}{L_k}+\frac{1}{L_m}\right]+\frac{T_s}{100}$ $\delta T_s\|_{BUCK}>\frac{2L_2(1-D)P_o}{V_l^2}+\frac{T_s}{100}-\frac{L_2}{n^2}D\left(1-D-\frac{1}{50}\right)\left(\frac{(n-1)^2}{L_k}+\frac{1}{L_m}\right)T_s$
Δi_ℓ	$\Delta i_\ell=\Delta i_{Lm}=\frac{V_\ell}{L_m}DT_s$	$\Delta i_\ell=\Delta i_{Lk}=\frac{(n-1)V_\ell}{nL_k}DT_s$
I_{k1}, I_{k2}	$I_{k2}=I_\ell-\frac{(n-1)V_\ell}{2nL_k}DT_s$ $I_{k1}=I_\ell+\frac{(n-1)V_\ell}{2nL_k}DT_s$	-
i_{S1} , i_{S2} In boost operating mode	$i_{S1}\|_{\min}=I_{m2}-I_{s2}$ $i_{S1}\|_{\max}=I_{s1}+I_{m1}$ $i_{S2}\|_{\min}=-(I_{s1}+I_{m1})$ $i_{S2}\|_{\max}=I_{s2}-I_{m2}$	$i_{S1}\|_{\min}=[(n-1)I_{k2}+I_{m2}]/n-I_{S2}$ $i_{S1}\|_{\max}=[(n-1)I_{k1}+I_{m1}]/n+I_{S1}$ $i_{S2}\|_{\min}=-[(n-1)I_{k1}+I_{m1}]/n-I_{S1}$ $i_{S2}\|_{\max}=-[(n-1)I_{k2}+I_{m2}]/n+I_{S2}$
i_{S1} , i_{S2} In buck operating mode	$i_{S1}\|_{\min}=-(I_{m1}+I_{s2})$ $i_{S1}\|_{\max}=I_{s1}-I_{m2}$ $i_{S2}\|_{\min}=I_{m2}-I_{s1}$ $i_{S2}\|_{\max}=I_{m1}+I_{s2}$	$i_{S1}\|_{\min}=-[(n-1)I_{k1}+I_{m1}]/n-I_{S2}$ $i_{S1}\|_{\max}=-[(n-1)I_{k2}+I_{m2}]/n+I_{S1}$ $i_{S2}\|_{\max}=[(n-1)I_{k1}+I_m]/n+I_{S2}$ $i_{S2}\|_{\min}=[(n-1)I_{k2}+I_{m2}]/n-I_{S1}$

9 Simulation Results

In order to reconfirm the obtained theoretical analyses and capability of making ZVS for the main switches with the zero input current ripple in the proposed topology, the simulation results in PSCAD/EMTDC software program are used in boost operating mode. The simulation results also can be extracted for buck operating mode. The used parameters in simulation considered as $f_s=50\,\text{kHz}$, $D=0.7$, $V_\ell=24\,\text{V}$, $L_2=40\,\mu\text{H}$, $L_m=96\,\mu\text{H}$, $L_k=54\,\mu\text{H}$, $\delta T_S=1.6\,\mu\text{sec.}$, $C_3=200\,\mu\text{F}$, $C_4=21\,\mu\text{F}$, $R_H=128\,\Omega$, $C_H=100\,\mu\text{F}$. The output power is equal to $P_H=50\,\text{W}$.

It is possible to stimulate the switches of the proposed topology by using pulse width modulation control method. For instance, the stimulation signal for switch S_4 is obtained by comparing the triangle carrier waveform (A_c) with the reference waveform (A_r) in a way that if $A_r > A_c$, the value of the stimulation pulse is equal to 1, otherwise it is equal to 0. After generation the fire pulse of the switch S_4, the pulse of the switch S_1 is generated by applying the delay time equal to δT_S. The switches of S_3 and S_2 act in a complementary method to the switches of S_4 and S_1, respectively. The stimulation pulse of the switches based on the pulse width modulation method is shown in Fig. 6. In addition, Fig. 7 shows the used blocks to generate stimulation pulse in the simulation.

There is other method to stimulate switches that has higher accuracy and leads to better performance of the converter. In this method, the phase shifts are considered for the switches pulses in a way that the fire pulses has to be as same as Fig. 2. This method is used in the simulation. The required phase shifts for the switches in the simulation are shown in Fig. 8. In this method, the values of dead times between the switches S_1 and S_2 in addition to the switches S_3 and S_4 based on (5), (14) and by considering the value of the parasitic capacitor equal to $C_1=C_2=0.0005\,\mu\text{F}$ is carefully adjusted. It is possible to consider the dead time equal to $T_{dead}=T_S/100$.

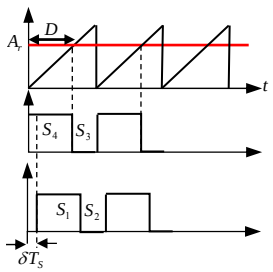

Fig. 6 Stimulation of the switches based on pulse width modulation method.

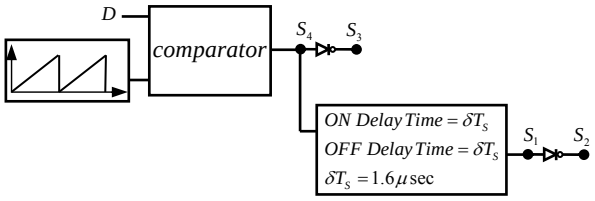

Fig. 7 Used blocks to generate stimulation pulses in the simulation results.

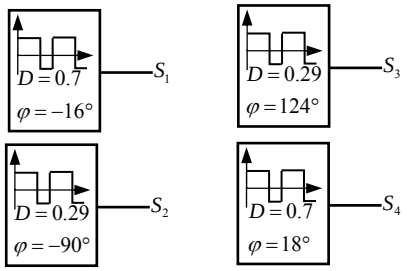

Fig. 8 Stimulation pulses based on phase shift method.

Figs. 9(a) and 9(b) show the capability of ZVS for the main switches S_1 and S_2. As shown in these figures, by turning on the auxiliary diodes of D_1 and D_2 their voltage (v_{S1} and v_{S2}) are equal to zero. In this condition, the trigger pulses of the switches of S_1 and S_2 are applied before the direction of the currents i_{S1} and i_{S2} have been changed. As a result, the ZVS is made for the main switches. Figs. 9(c) and 9(d) show the capability of the ZCS for the main switches of S_3 and S_4 in the turning off times. As shown in these figures, the voltage stress for the switches of S_3 and S_4 are half of the high voltage source (V_H) due to existing clamped diodes of D_7 and D_8.

The voltage and current values of the capacitor C_4 in steady state is shown in Fig. 10. According to Fig. 10 and by considering the ripple voltage value of ΔV_{C4} that is equal to $V_{C4}/100$, it is resulted that:

$$C_4 \frac{\Delta V}{\Delta T} = \int_0^{2\delta T_S} i_{L2} \tag{47}$$

$$C_4 \frac{V_{C4}/100}{2\delta T_S} = \frac{1}{2} I_{S2} \cdot 2\delta T_S \tag{48}$$

$$C_4 \frac{V_H/200}{2\delta T_S} = \frac{1}{2} I_{S2} \cdot 2\delta T_S \tag{49}$$

$$C_4 \frac{V_H/200}{2\delta T_S} = \frac{1}{2} \cdot \frac{V_H}{2L_2} \delta T_S \cdot 2\delta T_S \tag{50}$$

By considering $\delta T_S = 1.6\,\mu\text{sec}$. and according to the above equation, the value of the capacitor C_4 is determined as follows:

$$C_4 \frac{80/200}{2(1.6\mu)} = \frac{1}{2} \cdot \frac{80}{2(40\mu H)} (1.6\mu) \cdot 2(1.6) \tag{51}$$

By simplifying Eq. (51) C_4 is obtained equal to $21\,\mu\text{F}$.

In addition, the value of the capacitor C_4 is determined in a way that it is possible to avoid resonance between C_4 and L_2 while one of the auxiliary switches is turned on. In other word, it is obtained that:

$$T_r > 2T_s \tag{52}$$

$$\frac{f_s}{2} > \frac{1}{2\pi\sqrt{L_2 C_4}} \tag{53}$$

$$C_4 > \frac{1}{40\mu(50000\pi)^2} > 1.013\,\mu\text{F} \tag{54}$$

The capacitor voltage charging method is shown in Fig. 11.

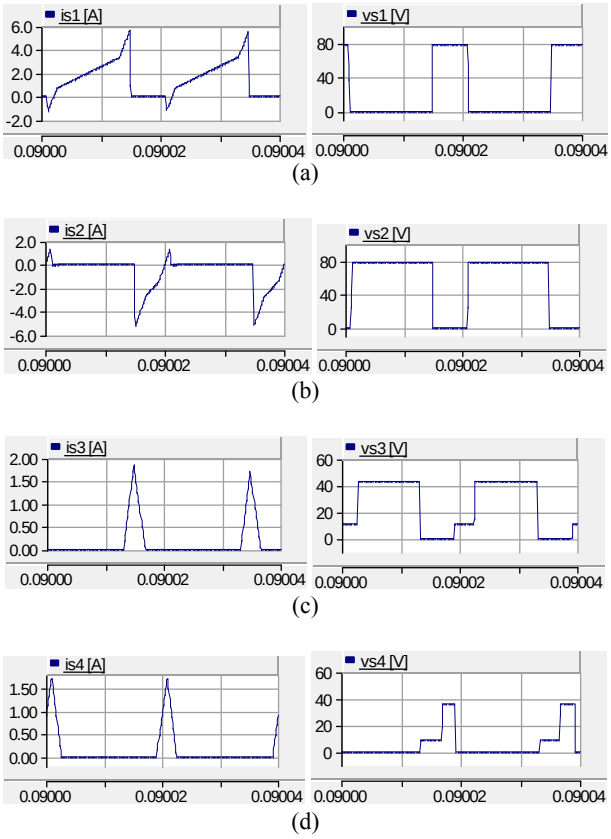

Fig. 9 Voltage and current of switches; (a) S_1; (b) S_2; (c) S_3; (d) S_4.

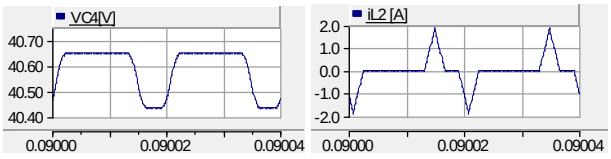

Fig. 10 Voltage and current waveforms of the capacitor C_4.

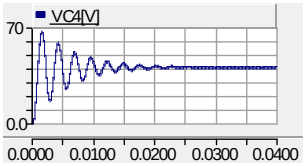

Fig. 11 Voltage waveform of the capacitor C_4.

Fig. 12 shows the transmission current from the input bridge in the boost operating mode. The current of i_T is equal to $-i_{Ls}$. According to Fig. 3, the input current of i_ℓ is equal to sum of the currents i_{Lm} and i_T. As shown in Fig. 12 and based on circuit's parameters, the sum of the currents i_T and i_{Lm} is always equal to the constant dc value in the steady state. As shown in Fig. 13, the input current ripple is equal to $i_\ell = 0.003A$. This value is lower than the input bridge current ripple $(i_{PS} = 4A)$. This point shows that it is possible to generate zero input current ripple without making any problem in ZVS and ZCS operating of the switches. This feature is obtained only by regulating the parameters of coupled inductor. In this condition, the value of the input current stress is reduced. As the capacitor and inductor are used in the input bridge, it is necessary to consider the switching frequency of the converter very higher than the resonance frequency $(1/\sqrt{L_S C_3})$ which is made by the resonance between the inductor L_S and capacitor C_3. As a result, the switching frequency is considered 5 times higher than the resonance frequency.

The efficiency of the proposed converter for boost operating mode by considering output power of $P_H = 50W$ is equal to $\eta = 0.986$. Fig. 13 shows the efficiency of the proposed converter in the boost operating mode for different output power. As mentioned before, in order to operate the converter at the ZVS state and increase the output power based on constant value of δT_S, the value of the inductor L_2 has to be decreased or based on the constant value of L_2 the value of δT_S has to be decreased (According to Fig. 5). In this section, by considering the constant value of $\delta T_S = 1.6\,\mu\text{sec}$. and by increasing the output power, the value of the inductor L_2 is only decreased. As shown in Fig. 13, the efficiency of the converter is higher than 98% for the power higher than 40 W. The values of the selected L_2 for using different powers in the ZVS operating modes of the converter are shown in Table 3.

Table 3 The values of the inductor L_2 for different output power.

$P_H = 10W$ $L_2 = 100\mu H$	$P_H = 20W$ $L_2 = 80\mu H$	$P_H = 30W$ $L_2 = 70\mu H$	$P_H = 40W$ $L_2 = 60\mu H$
$P_H = 50W$ $L_2 = 40\mu H$	$P_H = 60W$ $L_2 = 30\mu H$	$P_H = 70W$ $L_2 = 30\mu H$	$P_H = 80W, 90W, 100W$ $L_2 = 20\mu H$

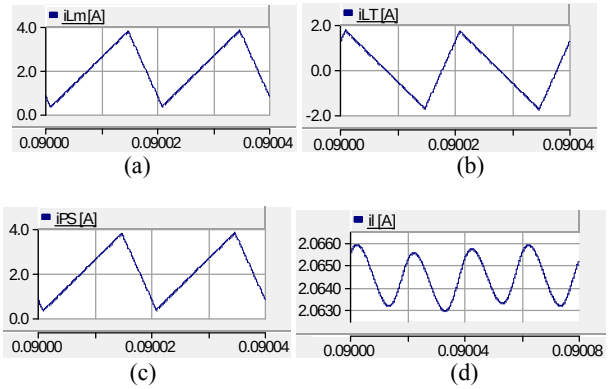

Fig. 12 The input bridge currents in boost operation; (a) i_{Lm}; (b) i_{LT}; (c) i_{PS}; (d) i_ℓ

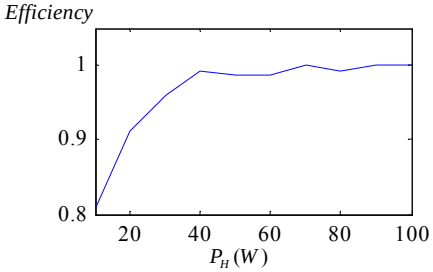

Fig. 13 The efficiency of the proposed converter based on different output power.

10 Conclusion

In this paper, a new dc-dc buck-boost converter with the capability of soft switching and zero input current ripple is proposed. In this topology, ZVS for the main switches of (S_1 and S_2) and ZCS for the auxiliary switches (S_3 and S_4) are always made. The circulating current is reduced because of operating the lossless active snubber. The proposed Topology in comparison with the conventional Topologies such as poly-phase needs lower number of elements to eliminate the input current ripple. The required conditions for soft switching operating mode and also for eliminating the input current ripple are obtained. Moreover, the equations of the voltage and current of all elements of the proposed topology are calculated in all operating modes. Finally, the correct operation of the proposed topology and also the given theoretical are reconfirmed by simulation results by using PSCAD/EMTDC software.

References

[1] D. S. Wijeratne and G. Moschopoulos, "A ZVS-PWM full-bridge converter with reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3501–3513, July 2014.

[2] I.O. Lee and G.W. Moon, "Soft-switching dc-dc converter with a full ZVS range and reduced output filter for high-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 112-122, Jan. 2013.

[3] R. Yang, H. F. Ding, Y. Xu, L. Yao, and Y. Meng. Xiang, "An analytical steady-state model of LCC type series–parallel Resonant converter with capacitive output filter," *IEEE Trans. Power Electron*., vol. 29, no. 1, pp. 328-338, Jan. 2014.

[4] B. Gu, J. Sh. Lai, N. Kees, and C. Zheng, "Hybrid Switching Full-Bridge DC–DC Converter With Minimal Voltage Stress of Bridge Rectifier, Reduced Circulating Losses, and Filter Requirement for Electric Vehicle Battery Chargers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1132-1144, March. 2013.

[5] X. Huang, F.C. Lee, *L. Fellow*, Q. Li, and W. Du, "High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 1915-1922, June. 2016.

[6] K. Jin, and C. Liu, "A Novel PWM High Voltage Conversion Ratio Bidirectional Three-Phase DC/DC Converter With Y–Δ Connected Transformer," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 81–88, Jan. 2016.

[7] E. Babaei, M.E. Seyed Mahmoodieh, and M. Sabahi, "Investigating buck dc-dc converter operation in different operational modes and obtaining the minimum output voltage ripple considering filter size," *Journal of Power Electronics*, vol. 11, no. 6, pp. 793-800, Nov. 2011.

[8] E. Babaei and M. E. Seyed Mahmoodieh, "Calculation of output voltage ripple and design considerations of Sepic converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1213-1222, March 2014.

[9] E. Babaei, M. E. Seyed Mahmoodieh, and H. Mashinchi Mahery, "Operational modes and output voltage ripple analysis and design considerations of buck-boost dc-dc converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 381-391, Jan. 2012.

[10] M. R. Mohammadi and H. Farzanehfard, "A New Family of Zero-Voltage-Transition Nonisolated Bidirectional Converters With Simple Auxiliary Circu*it," IEEE Trans. Ind. Electron.,* vol. 63, no. 3, pp. 2-9, March 2016.

[11] F. M. Ibanez, J. M. Echeverria, D. Astigarraga, and L. Fontan, "Soft-switching forward DC–DC converter using a continuous current mode for electric vehicle applications," *IET Power Electronics.*, vol. 8, no. 10, pp. 1978–1986, 2015.

[12] T. F. Wu, Y. C. Chen, J. G. Yang, and C. L. Kuo, "Isolated bidirectional full-bridge DC-DC converter with a flyback snubber," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1915–1922, Jul. 2010.

[13] T. Nouri, S. H. Hosseini, E., Babaei, and J., Ebrahimi, "Interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell," *IET Power Electron.*, vol. 8, no. 2, pp. 175–189, 2014.

[14] D. Y. Jung, S. H. Hwang, Y. H. Ji, J. H. Lee, Y-C. Jung, and C-Y. Won, "Soft-switching bidirectional DC/DC converter with a LC series resonant circuit," *IEEE Trans. Power Electron.*, vol. 28, no. 4, April 2013.

[15] H.L. Do "Nonisolated Bidirectional Zero-Voltage-Switching DC–DC Converter*" IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2563-2569, Sep. 2011.

[16] J. Zhang, "Bidirectional DC-DC power converter design optimization, modeling and control," PHD Thesis, Virginia Polytechnic Institute and State University, 2008.

[17] J. W. Yang and H. L. Do, "Soft-switching bidirectional dc-dc converter using a lossless active snubber," *IEEE Trans. Circuits and Systems*, vol. 61, no. 5, pp. 1588-1596, May 2014.

[18] L. Jiang, C. C. Mi, S. Li, M. Zhang, X. Zhang, and C. Yin, "A novel soft-switching bidirectional dc-dc converter with coupled inductors," *IEEE Trans. Ind. Appl.*, vol. 49, no. 6, pp. 2730-2740, Nov./Dec. 2013.

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