A New Topology for Interline Dynamic Voltage Restorer Based on Direct Three-Phase Converter

E. Babaei*(C.A.) and M. R. Farzinnia*

Abstract: In this paper, a new topology for Interline Dynamic Voltage Restorer (IDVR) is proposed. This topology contains two direct three-phase converters which have been connected together by a common fictitious dc-link. According to the kind of the disturbances, both of the converters can be employed as a rectifier or inverter. The converters receive the required compensation energy from the gird through the direct link which is provided by the dual-proposed switches. Due to the lack of the huge storage elements, the practical prototype of the proposed topology is more economical in comparison with the traditional structure. Moreover, compensating for long time duration is possible due to the unlimited eternal energy which is provided from the grids. The low volume, cost and weight are the additional features of the proposed topology in comparison with traditional types. This topology is capable to compensate both of the balanced and unbalanced disturbances. Furthermore, restoring the deep sags and power outages will be possible with the support from the other grid. Unlike the conventional topologies, the capability of compensation is independent from the power flow and the power factor of each grid. The performance of the proposed IDVR topology is validated by computer simulation with PSCAD/EMTDC software.

Keywords: Cycloconverter, IDVR, Voltage Quality, Voltage Sag.

1 Introduction

Nowadays, a wide application of electronic devices in the industrial centers, medical centers and etc. has caused the power quality to be considered as one of the most important issues in the power system studies. Any disturbance in the voltage including sags, swells, harmonics and flickers affect the power quality [1-3]. Voltage disturbances cause inappropriate operation of sensitive loads, heat generating in electrical machinery and control systems faults [4-5]. Since the voltage disturbances are unpredictable, the compensator response time should be low. The power electronic devices due to the high speed performance are proper choices for compensation [6].

Dynamic voltage restore (DVR) is one of the series-connected custom power devices that protect the sensitive loads against voltage disturbances [5]. DVRs inject the required voltage of compensation through the injection transformers which are placed in series with the grid lines. Since in the conventional topologies of DVR the energy storage elements are responsible to provide the required energy, so, the DVR is unable to restore the voltage for long time intervals [5-8].

The IDVR is a kind of expanded DVR topologies that compensate two or more grids by using a common dc-link. Fig. 1 shows a conventional topology of IDVR which consists of two compensator block. In order to power exchange, the compensator is inserted back to back.

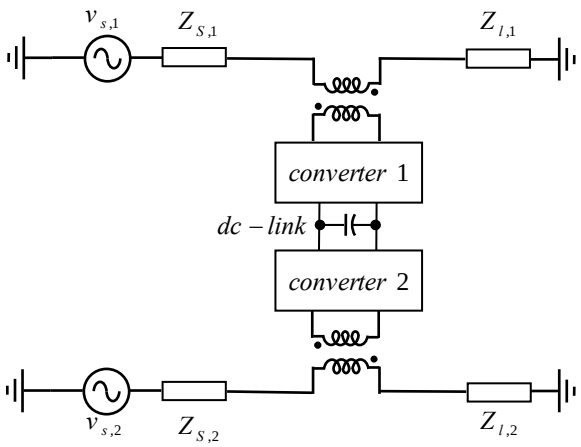

Fig. 1 Conventional topology for IDVR.

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In addition, a common dc-link has been considered to provide a bidirectional power flow path between the equipment. Coincide with the perturbation occurrence; the compensator which is connected to the disrupted grid starts to restore the voltage profile. On the other hand, the remained compensator provides the required energy by operating as a rectifier [9]. Unlike DVR, the large energy storage elements can be eliminated from the IDVR structures due to the direct energy harvesting from the grid(s). Apart from this feature, the IDVR be capable to restore the disturbance for long time intervals [10]. There are several studies accomplished for IDVR which present new control methods to improve the operation [9-11] but the number of the papers which are focused on the IDVR topology is so limited. It is noticeable that the range of the compensation capability of the IDVR is strongly depended on the current and power factor of each grid [9-11]. Unlike the IDVR, there are several studies performed for DVR to present new control methods and topologies. The presented topologies for DVR can be classified into two categories. The first type is based on the conventional structure and uses the storage elements as an energy provider [4]. The second category includes the topologies which are directly connected to the grid and receives the required energy through this connection.

In [12], the presented topology for single-phase DVR is based on a direct ac/ac conversion capable to proper compensate different kind of the turbulence. In order to protect the voltage from any kinds of symmetric and asymmetric disturbances, a three-phase DVR has been presented by using an ac/ac converter in [13]. In [14], a new kind of DVR based on voltage regulator has been presented. However this topology has less number of switches in comparison with the traditional topologies but the number of transformers has been increased. In [15], the presented topology is based on reduced-order matrix converter and generates the required compensation voltage by decomposing into positive and negative sequences. In the presented topology in [16], the required energy of compensation the voltage sag is supplied from two other phase of the grid. In [17], the presented topology for a single-phase DVR can limit down-stream fault currents in addition the voltage compensation.

However the second category contains the topology which is capable to restore the voltage for long-time intervals but, the range of the compensation capability is strongly depended on the supplied voltage amplitude [12-14]. In other words, the compensation ability is extremely reduced under severe disturbance condition like deep sags.

As mentioned unlike the DVR, the topology of the IDVR has been remained unchanged. Inspired by the evolution of the DVR structures, a new topology for IDVR based on direct ac/ac conversion is proposed. Despite the conventional topologies of IDVR, the required energy is directly supplied by the grids and the needing for the massive storage elements such as dc-link capacitor is eliminated in the proposed topology. As a result, the proposed topology is able to compensate severe voltage sags or even power outage in one of the grids without any time limitation. On the contrary the conventional ac/ac converters, unidirectional switches are used in this topology instead the bidirectional switches.

At first, the proposed topology for IDVR is described. Then, a proper control method for voltage compensation and control of converters is explained. Moreover, the range of the compensation capability of the IDVR is calculated. In order to verify the claimed features and correct operation, the simulation results for different disturbance condition is presented. To prove the correctness operation of the proposed topology and control method, the simulation results by using PSCAD/EMTDC software are used.

2 Proposed Topology

Fig. 2 shows the block diagram of the proposed topology for IDVR. The implemented converters can operate as rectifier or inverter according to the grids conditions. Dual purposed switches are employed to meets two objectives: to create the connection between the grid and the converters and providing the bypass route in parallel to the injection transformers. When each of the grids be in disturbance condition (assume, grid 1) the next converter (connected to grid 2) starts to operate in rectifier mode. Therefore, the mentioned converter is directly connected to the grid through the dual purpose switches. Afterward, the converter which is placed in the disturbance side generates the required compensation voltage by using the supplied dc voltage. It is noticeable that the dual purpose switches in disturbance side breaks the bypass route and isolates the converter from the grid. Because of the high switching frequency, the produced voltage contains high-order harmonics, which should be eliminated. Therefore the low-pass filter is used behind the injection transformers.

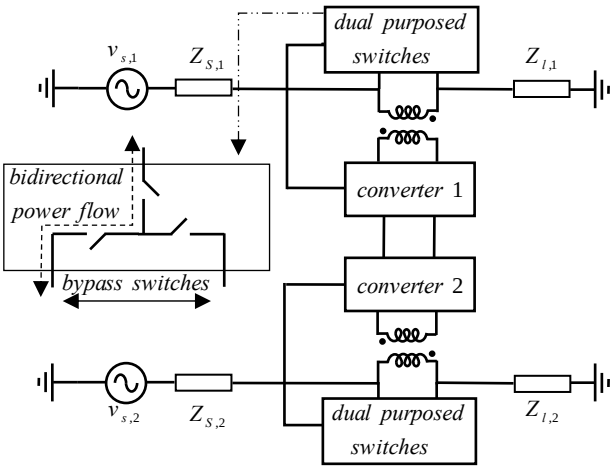

Fig. 2 Block diagram of proposed topology for IDVR.

The detailed structure of the proposed IDVR is illustrated in Fig. 3. In this figure, $S_{bypass,1}$ and $S_{bypass,2}$ switches are used to create bypass when the corresponding grids are under normal conditions. $S_{a,k}$, $S_{b,k}$ and $S_{c,k}$ (for k = 1, 2) switches are used to connect (isolate) the converter to (from) the grid. $S_{1,k}$, $S_{2,k}$, … and $S_{6,k}$ switches are the components of each converter. $S_{break,k}$ switches are used to separate injection part from converter when the converter operates as a rectifier. The inductor L_f and the capacitor C_f are used as the low-pass filter. Operation status of the components of the proposed topology is presented in Table 1.

In the proposed topology, in addition to casual role of bypass switches, $S_{bypass,k}$ switches perform supplement role to connect and disconnect the converter to the grid. When $S_{bypass,k}$, $S_{a,k}$, $S_{b,k}$ and $S_{c,k}$ switches are turned on, each converter can connect to the grids with bidirectional power flow.

When each of the converters operates in rectifier mode, the converter connects to the grid according to the mentioned manner. In order to separate the injection parts from the converter and avoid unwanted current flow in the rectifier mode, $S_{break,k}$ switches are used in the proposed topology. If $S_{break,k}$ be turned off, the current flow in the filter part will equal to zero. In order to isolate the converter from the grid in the inverter mode, $S_{bypass,k}$, $S_{a,k}$, $S_{b,k}$ and $S_{c,k}$ switches are turned off. As a result, the required voltage for compensation can be injected through series transformers. The relation between the grid, injected and load voltages can be considered as follows:

$$\begin{aligned} v_{L,ak} &= v_{G,ak} + v_{D,ak} \\ v_{L,bk} &= v_{G,bk} + v_{D,bk} \quad for\ k = 1,2 \\ v_{L,ck} &= v_{G,ck} + v_{D,ck} \end{aligned} \tag{1}$$

where, $v_{L,ak}$, $v_{L,bk}$ and $v_{L,ck}$ denote the load voltages of phases *a*, *b* and *c* respectively. $v_{G,ak}$, $v_{G,bk}$ and $v_{G,ck}$ are the grid voltages of phases *a*, *b* and *c*, respectively $v_{D,ak}$, $v_{D,bk}$ and $v_{D,ck}$ are the injected voltages to phases *a*, *b* and *c*, respectively.

When each of the grids is under disturbance, the required voltage for compensation is produced and injected to the grid voltage. The relation between the produced voltages and injected voltage can be expressed as follows:

$$\begin{aligned} v_{D,ak} &= nqv_{o,ak} \\ v_{D,bk} &= nqv_{o,bk} \quad for\ k = 1, 2 \\ v_{D,ck} &= nqv_{o,ck} \end{aligned} \tag{2}$$

In the above equations, n and q are considered as the voltage transfer ratio of the injection transformer and the low-pass filter, respectively. $v_{o,ak}$, $v_{o,bk}$ and $v_{o,ck}$ represent the produced voltages by the converters.

In the proposed topology, the required energy for compensation is directly provided by the grids.

Therefore, there is no need to any large dc-link capacitors in this topology. Due to the high volume, weight and cost of dc-link are considered as a disadvantage for conventional topology of IDVR. In order to eliminate the voltage ripple and spike caused by each converter, a capacitor is used between the converters. It should be mentioned that the capacitance of the used capacitor (say *10 μF*) is very low in comparison with the dc-link capacitors.

A comparison of the required number of switches between the proposed topology and several conventional topologies of DVR based on direct ac/ac conversion has been presented in Table 2. According to the table, the number of required switches in the proposed topology is reduced in comparison with using two independent DVR for two grids. Unlike the DVR, the capability of the compensation of the proposed topology is not related to the grid voltage which is under disturbance. Therefore, the restoration capability is not reduced under severe sags and swells.

3 Control Method

Control strategy of the proposed topology is adopted from the presented control method in [18]. As explained in the previous section, the converters may operate as inverter or rectifier depends on different grid's situations (Table 1). In this section, the operation principles of the converters in rectifier and inverter modes are separately explained. Moreover, the strategy for voltage disturbance detection and generating reference signal is discussed.

3.1 Rectifier Mode

In order to provide the required energy and voltage for compensating in the proposed topology, one of the converters should play the rectifier role. Grid 1 is selected as the case of study to explain the rectifier mode. However, all of the obtained results for grid 1 can be referred to grid 2. The voltages of phases in grid 1 in the symmetric condition can be written as follows:

$$\begin{aligned} v_{G,a1}(t) &= V_{G,m1}\sin(\omega t) \\ v_{G,b1}(t) &= V_{G,m1}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_{G,c1}(t) &= V_{G,m1}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{3}$$

In the above equations, $v_{G,a1}$, $v_{G,b1}$ and $v_{G,c1}$ denote the voltages of phases *a*, *b* and *c* in the grid 1, respectively. Also, ω and $v_{G,m1}$ are the angular frequency and amplitude of voltages, respectively.

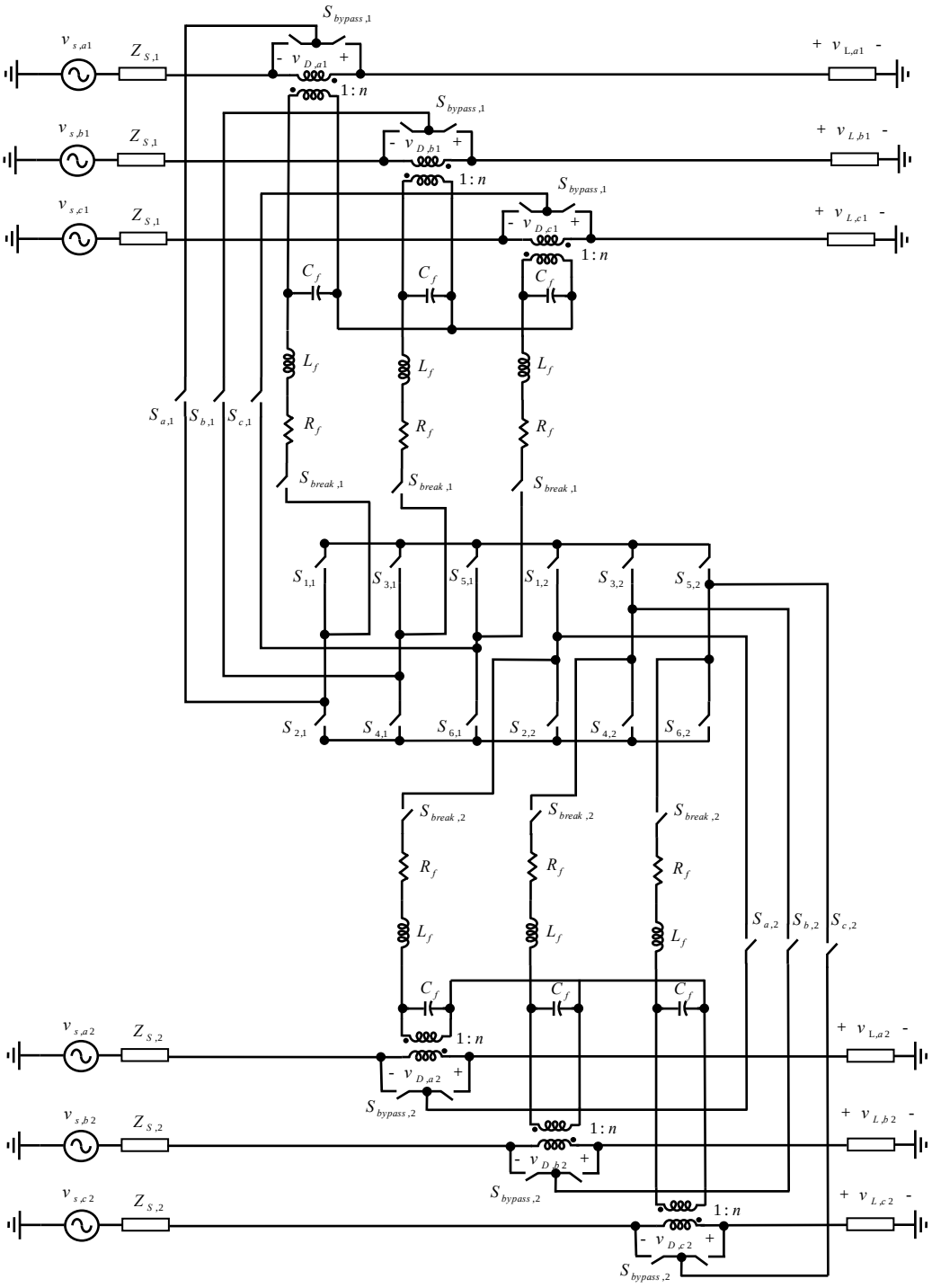

Fig. 3 The proposed topology for IDVR.

Table 1 The operation of IDVR components in the expected conditions.

Condition of Grids		**Operation of Components in Grid 1**			**Operation of Components in Grid 2**		
Grid 1	Grid 2	$S_{bypass,1}$	$S_{a,1}$, $S_{b,1}$, $S_{c,1}$	Converter 1	$S_{bypass,2}$	$S_{a,2}$, $S_{b,2}$, $S_{c,2}$	Converter 2
normal	normal	on	off	off	on	off	off
normal	disturbance	on	on	rectifier	off	off	inverter
disturbance	normal	off	off	inverter	on	on	rectifier

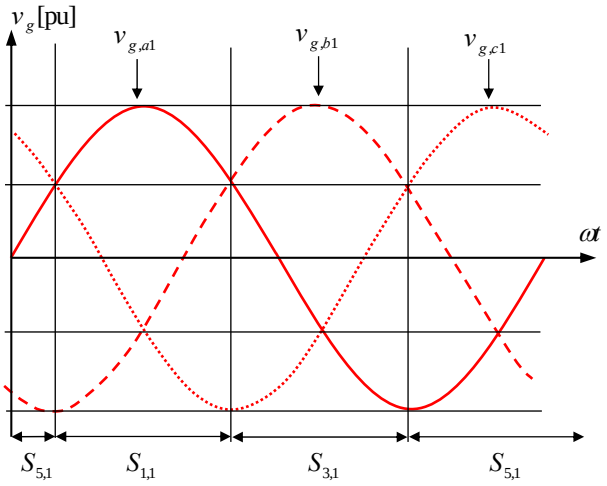

Fig. 4 The rectifier switching, according to the waveforms of the phase voltage in grid 1.

Table 2 Comparison the component of the proposed topology with the presented topologies.

Topology	Number of the Required Switches	
	Single Grid	Dual Grid
In [12]	18	36
In [13]	30	60
In [16]	30	60
Proposed	-	36

Table 3 The output voltages of the converter for different switching configurations.

State of Operation	On Switches	Line Voltages of Converter Output		
		$v_{o,ab}$	$v_{o,bc}$	$v_{o,ca}$
I	$S_{1,k}$, $S_{4,k}$, $S_{5,k}$	v_{dc}	$-v_{dc}$	0
II	$S_{1,k}$, $S_{3,k}$, $S_{6,k}$	0	v_{dc}	$-v_{dc}$
III	$S_{2,k}$, $S_{3,k}$, $S_{5,k}$	$-v_{dc}$	0	v_{dc}
IV	$S_{2,k}$, $S_{4,k}$, $S_{5,k}$	0	$-v_{dc}$	v_{dc}
V	$S_{1,k}$, $S_{4,k}$, $S_{6,k}$	v_{dc}	0	$-v_{dc}$
VI	$S_{2,k}$, $S_{3,k}$, $S_{6,k}$	$-v_{dc}$	v_{dc}	0

Fig. 4 shows the voltage waveforms of the phase voltages along with the participation of switches in a period. As shown in the figure, the phase which has the high voltage in comparison with the other phases has been connected to the positive pole of the common link via the proper switching. Similarly, the phase which has the lowest voltage is connected to the negative pole of the common link. In order to connect each of the phases to the positive pole of the link, $S_{1,k}$, $S_{3,k}$ and $S_{5,k}$ switches are employed. Moreover, each of the phases can be connected to the negative pole through $S_{2,k}$, $S_{4,k}$ and $S_{6,k}$ switches.

3.2 Inverter Mode

In order to produce the required compensation voltage in the proposed topology, the converter should operate as an inverter. The presented method in [19] has been implemented as the operation algorithm of the inverter. In the inverter mode, the converter has eight possible switching configurations which, two of them cause zero voltage at output and can be neglected. Table 3 presents the output voltages of the converter for six mentioned configurations of switching.

The switching period covers six time intervals which are marked by t_i (for i=1, 2, …, 6). Each of the mentioned time duration is assigned to one of the sextuplet switching configurations. In other word, all of the considered switching configurations participate in each switching period. Due to simplify the equations and isochronisms, the switching period (T_s) is divided into two equal parts and each part covers three numbers of the exclusive switching configuration which are explained as follows:

$$\frac{T_s}{2} = t_1 + t_2 + t_3 \tag{4}$$

$$\frac{T_s}{2} = t_4 + t_5 + t_6 \tag{5}$$

It is clear that the sextuplet time intervals t_i should be greater than or equal to zero. As a result, the following inequality is required to execute for each of t_1 to t_6 time intervals. As a result, by considering Eqs. (4) and (5), the following inequality is obtained:

$$0 \le t_i \le \frac{T_s}{2} \quad for \quad i = 1,2,\cdots,6 \tag{6}$$

Given the balancing of three-phase load, the following equations are established between lines and phases voltages:

$$\begin{aligned} v_{o,ab} &= v_{o,a} - v_{o,b} \\ v_{o,bc} &= v_{o,b} - v_{o,c} \\ v_{o,ca} &= v_{o,c} - v_{o,a} \end{aligned} \tag{7}$$

In the above equations, $v_{o,a}$, $v_{o,b}$ and $v_{o,c}$ are denotes the phase voltages of the output.

Considering Eq. (7) and the generated line voltages by different switching configurations which are presented in Table 3, the output voltages for triple phases can be obtained. Fig. 5 shows the generated phase voltages per each switching period. According to the figure, resultant output voltage of each phase in a switching period is equal to average of generated voltage caused by different switching arrangements. Furthermore, the average of generated voltages among

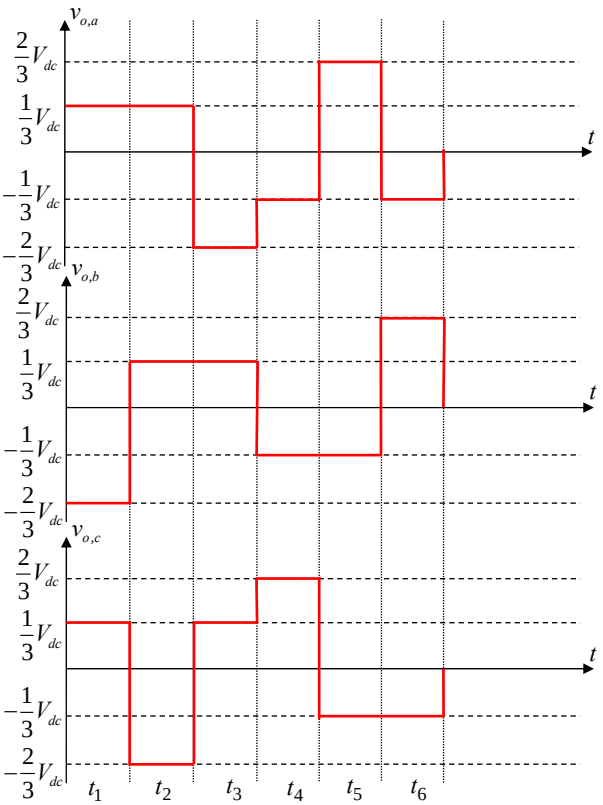

Fig. 5 Generated voltages during the switching period.

first half and second half of switching period should be equal to half of the desired output voltages. In the other word, the amounts of t_i (for i=1, 2, …, 6) should satisfy the recent conditions to obtain the desired voltages.

Attend to generated voltage shown in Fig. 5, the average of generated line voltage is calculated as follows:

$$v_{o,ab} = \frac{v_{dc}}{T_s}(t_1 - t_3 + t_5 - t_6)$$

$$v_{o,bc} = \frac{v_{dc}}{T_s}(-t_1 + t_2 - t_4 + t_6) \quad (8)$$

$$v_{o,ca} = \frac{v_{dc}}{T_s}(-t_2 + t_3 + t_4 - t_5)$$

To calculate the values of t_1 to t_6, six independent equations are required. Considering Eq. (8), just two independent equations can be achieved. As noted, the average of generated voltages during first and second half of switching period should be equal to half of the desired voltage. As a result, the obtained equation in Eq. (8) can be expanded as follows:

$$\frac{v_{o,ab}}{2} = \frac{v_{dc}}{T_s}(t_1 - t_3) \quad (9)$$

$$\frac{v_{o,ab}}{2} = \frac{v_{dc}}{T_s}(t_5 - t_6) \quad (10)$$

$$\frac{v_{o,bc}}{2} = \frac{v_{dc}}{T_s}(-t_1 + t_2) \quad (11)$$

$$\frac{v_{o,bc}}{2} = \frac{v_{dc}}{T_s}(-t_4 + t_6) \quad (12)$$

Considering Eqs. (4), (5), (9), (10), (11) and (12), the following equations can be obtained:

$$\begin{bmatrix} 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ -1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \\ t_5 \\ t_6 \end{bmatrix} = \begin{bmatrix} \frac{v_{o,ab}}{2v_{dc}} \\ \frac{v_{o,ab}}{2v_{dc}} \\ \frac{v_{o,bc}}{2v_{dc}} \\ \frac{v_{o,bc}}{2v_{dc}} \\ \frac{1}{2} \\ \frac{1}{2} \end{bmatrix} T_s \quad (13)$$

By solving the above equation and considering Eq. (7), the values of t_1 to t_6 are calculated as follows:

$$t_1 = \frac{T_s}{6}\left(1 + \frac{v_{o,a} - 2v_{o,b} + v_{o,c}}{v_{dc}}\right)$$

$$t_2 = \frac{T_s}{6}\left(1 + \frac{v_{o,a} + v_{o,b} - 2v_{o,c}}{v_{dc}}\right)$$

$$t_3 = \frac{T_s}{6}\left(1 + \frac{-2v_{o,a} + v_{o,b} + v_{o,c}}{v_{dc}}\right) \quad (14)$$

$$t_4 = \frac{T_s}{6}\left(1 + \frac{-v_{o,a} - v_{o,b} + 2v_{o,c}}{v_{dc}}\right)$$

$$t_5 = \frac{T_s}{6}\left(1 + \frac{2v_{o,a} - v_{o,b} - v_{o,c}}{v_{dc}}\right)$$

$$t_6 = \frac{T_s}{6}\left(1 + \frac{v_{o,a} - 2v_{o,b} + v_{o,c}}{v_{dc}}\right)$$

In the balanced condition, the output voltages of the converter can be assumed as follows:

$$v_{o,a}(t) = V_{o,m}\sin(\omega t)$$

$$v_{o,b}(t) = V_{o,m}\sin\left(\omega t - \frac{2\pi}{3}\right) \quad (15)$$

$$v_{o,c}(t) = V_{o,m}\sin\left(\omega t + \frac{2\pi}{3}\right)$$

In the above equation, $V_{o,m}$ is the maximum possible amplitude of the output voltages for each phase.

By placement the Eq. (15) into Eq. (14), the results are obtained as follows:

$$t_i = \frac{T_s}{6}\left[1 - \frac{3V_{o,m}\sin\left(\omega t - \frac{2i\pi}{3}\right)}{v_{dc}}\right] \quad (16)$$

$$for \quad i = 1,2,3$$

$$t_i = \frac{T_s}{6}\left[1 - \frac{3V_{o,m}\sin\left(\omega t - \frac{2(i-2)\pi}{3}\right)}{v_{dc}}\right] \quad (17)$$

$$for \quad i = 4,5,6$$

As previously mentioned, the calculated time segments should not be a negative value. By considering the recent condition, amount of $V_{o,m}$ should be considered as follows:

$$\frac{v_{o,m}}{v_{dc}} \le \frac{1}{3} \quad (18)$$

The above inequality explains the limitation of the voltage amplitude generated by the converter. As explained in Eq. (18), the amount of maximum amplitude producible is directly related to the range of the dc voltage.

3.3 Disturbances Detection and Reference Generation

The processes of disturbance detection and generating the reference signal have been shown in Fig. 6. According to the figure, the measured voltages for three phases of the grid are converted into two stationary phases of $\alpha\beta$ which have been shown with $v_{G,\alpha k}$ and $v_{G,\beta k}$ (for $k = 1, 2$). Afterward, two phases of $\alpha\beta$ are converted into two synchronous phases of dq, which are marked with $v_{G,dk}$ and $v_{G,qk}$. After subtracting the measured component from the assumed reference voltages ($v_{L,dk}^{ref}$ and $v_{L,qk}^{ref}$), according to inequality which is explained in Eq. (19), if the amount of sag or swell is more than the respected value, IDVR would start to compensate. According to the grids conditions, operation modes of each converter are determined. The result of subtraction is transformed to the stationary frame of $\alpha\beta$ and it is transformed to the three-phase signal, which are shown with $v_{D,ak}^{ref}$, $v_{D,bk}^{ref}$ and $v_{D,ck}^{ref}$. The obtained three-phase signals are the required amount of voltage for compensation. Finally, the amounts of t_1 to t_6 are calculated by the obtained equalities, according to Eq. (14).

$$if \ \sqrt{(v_{G,d} - v_{G,d}^{ref})^2 + (v_{G,q} - v_{G,q}^{ref})^2} \ge 0.02 \quad (19)$$
$$then \ \ detect = 1 \ else \ \ detect = 0$$

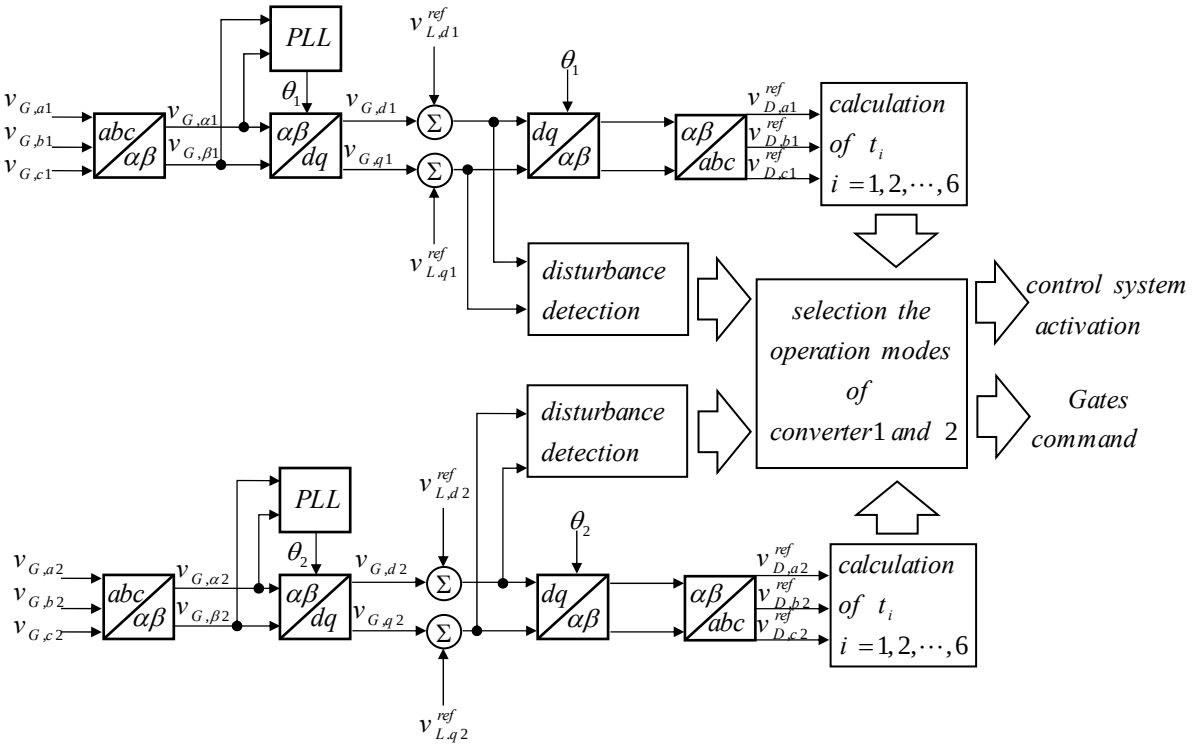

Fig. 6 Block diagram of the control method.

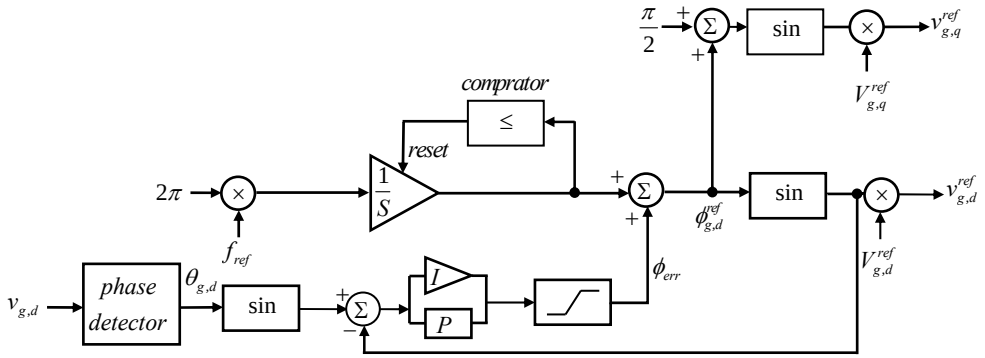

Fig. 7 Block diagram of the reference signal extraction.

Fig. 7 illustrates the method of extraction the reference signals ($v^{ref}_{L,d}$ and $v^{ref}_{L,q}$) from the grid voltages (v_g). The aim of the intended control part is generating the sinusoidal signals in phase with the grid voltage signal. As described previously, three phase voltage signals of the grid is transformed to *dq* synchronous frame. Since the obtained signals $v_{g,d}$ and $v_{g,q}$ are perpendicular, it is sufficient to consider one of the mentioned signal as the input of the control part. In the shown block diagram, $v_{g,d}$ is selected as the input variable. Initially, the phase angle of the input signal has been detected and the result is marked by $\theta_{g,d}$.

In order to prevent the errors caused by high-order harmonics, an additional low-pass filter should be applied in the phase detector block. Simultaneously, the next block produces a sinusoidal signal with unit amplitude which is in phase with the input signal. In order to lock the phase angle and Synchronization, the resultant signal is compared with the final form of the reference signal. The angular frequency of the desired reference signal should be a fixed amount which is equal to the nominal parameter of the grid. The comparator is responsible to react when the calculated phase is upper than 2π . Finally, the obtained reference phase angle is delivered to sinusoidal function and the result multiplied by appropriate amplitude.

Fig. 8 shows the scheme of the bypass switches with the injection transformer. According to the figure, the bypass switches are turned off while the voltage injection. When the turbulence is over, the bypass switches should be turned on. It should be noted that the voltage of the capacitor is remained after the compensating especially when the break switches isolate the filter part. This remained voltage can damages the switches while they are started to bypassing the injection transformer. Therefore, a proper switching control method for the bypass and the break switches should be considered. For this purpose, the residual voltage of the capacitor should be discharged.

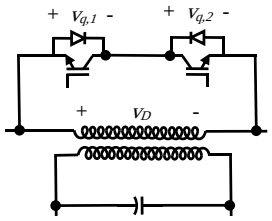

Fig. 8 scheme of the bypass switches with the injection transformer

In order to overcome the problem, an additional mode after finishing the compensation is considered. In this mode which is called “evacuation”, the bypass and break switches are not changed their states and the IDVR continue the injection but, the amplitude of the reference signal is reduced. By reducing the amount of reference signal, the amplitude of the injected voltage is consequently reduced. When the amplitude of injected voltage has been decreased, the bypass switches are activated while the break switches are turned on yet. In the last section of the evacuation, the reference voltage is biased on the zero voltage and the converter connects all the triple output to each other. Then, the break switches are turned off while the residual voltage of capacitors is in the allowable range.

By considering the non-ideality, the conductivity resistance of the switches should be noticed. For this reason the set of the switches and the capacitor can be modeled as two parallel impedances when the grid is under normal condition. The conductive resistance of the switches approximately are equal to several tens milliohm. The impedance of the capacitor in parallel with the switches is too greater than in comparison with the switches resistance. Therefore the impedance of the set can be considered equal to the switches resistance. So, the used switches for bypass are able to conduct the nominal current of the loads.

4 Simulation Results

In order to validate the acclaimed capability, the simulation results of the proposed IDVR by PSCAD/EMTDC software are presented. In this case

of simulation the grid 1 is assumed under disturbances and the grid 2 is in the normal condition.

The parameter of simulated system is presented in Table 4. The parameters of filter are selected so that the filter eliminates the high frequency components of voltage which have the minimum effect on the main harmonic. For this purpose, the cut-off frequency of the filter has been assumed ten times greater than the fundamental frequency.

Table 4 The Parameter of the simulated system

Parameters		Values
Grids 1 and 2	Voltage amplitude	$110\sqrt{2}V$
	frequency	$60Hz$
Load	resistance	100Ω
	inductance	$20mH$
	frequency	$60Hz$
Filters	inductance	$10mH$
	capacitor	$10\mu F$
	resistance	10Ω
Injection Transformers	Turns ratio	1 : 2
	leakage inductance	$1.5mH$
Switching Frequency		$10kHz$

To view the results of performance of IDVR, the grid voltage and the load voltage are compared under intentional disturbances.

Fig. 9 shows compensation under the voltage sag condition. As shown in the figure, in time interval between 0 and 0.01 sec., the grid voltage is in the normal condition and the injected voltage to the grid is zero. In the time interval between 0.01 and 0.08 sec. the voltage sag occurs. Amount of the voltage sag is equal to 0.35 pu. As the voltage disturbance happens, IDVR starts to compensate. As expected, the amount of the injected voltage is equal to the voltage sag. Therefore, the load voltage is properly compensated. At the beginning of compensation, the oscillation of the injected voltage is caused by the transient state which is damped in short time interval.

The simulation results for the voltage swell have been shown in Fig. 10. In the first half-period, the grid voltage is in the normal condition. At time 0.01 sec., the voltage swell occurs. The amount of the voltage swell is equal to 0.60 in the balanced condition. In the time interval between 0.01 and 0.08 sec., the required compensation voltage is produced by IDVR. It is clear that, the injected voltage has 180 degree phase difference with the grid voltage because of the swell condition. The simulation results indicate high speed response of the IDVR.

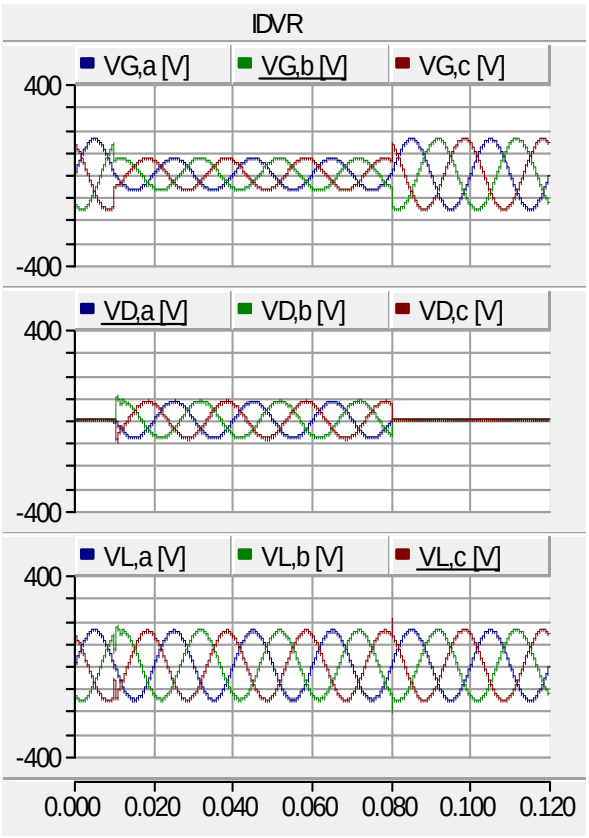

Fig. 9 Simulation results for the voltage sag.

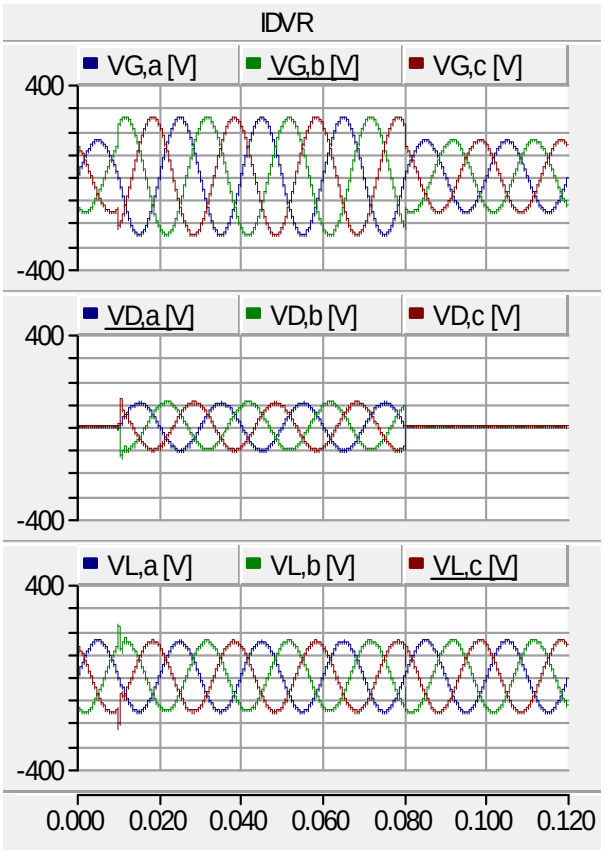

Fig. 10 Simulation results for the voltage swell.

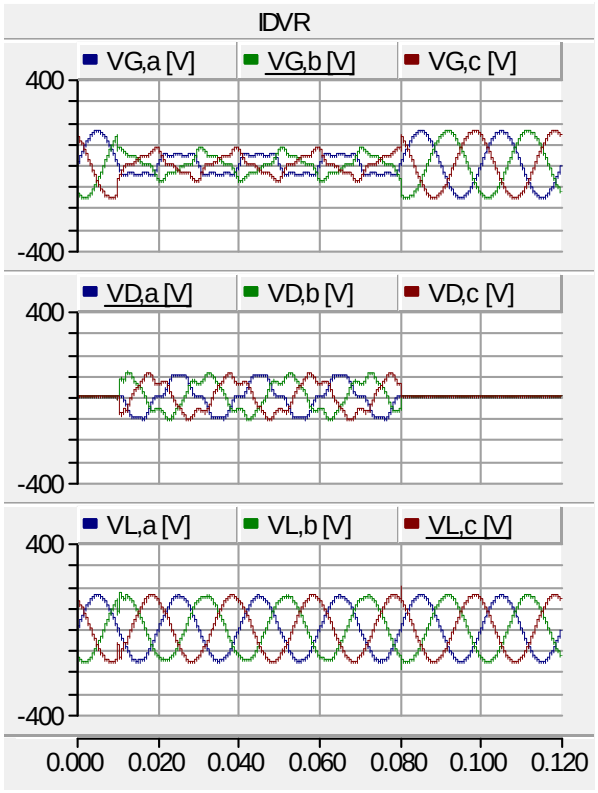

Fig. 11 Simulation results for presence of the annoying harmonics

Fig. 11 shows the simulation results in presence of the annoying harmonics. At first half-period, the grid voltage is in the normal condition. In the time interval between 0.01 and 0.08 sec., third and fifth harmonics are added to the grid voltage and the fundamental harmonic involves sag. Amplitudes of the third and fifth harmonics are 0.1 pu and 0.08 pu, respectively. Also the amount of the fundamental harmonic sag is 0.35 pu. In order to compensate, the injected voltage should contain subsidiary harmonics. Therefore, the injection filter should transfer the required high-order components of the grid voltage while compensation. In the other words, range of the cutoff frequency of the filter should be higher than the highest frequency of the voltage components which are considered to compensate

Fig. 12 shows the results of Fast Fourier Transform (FFT) for voltages of the grid and the load. As claimed, the grid voltage is contaminated by third and fifth harmonics. Also, the main harmonic is less than nominal amount. In the absence of compensator, this condition will cause disorder in electrical machines operation or damage to computer systems. After injection the voltage, high-order harmonics have been eliminated and the domain of main harmonic has been improved. As a result, the sensitive loads will be safe from harmonic disturbances by using the proposed topology.

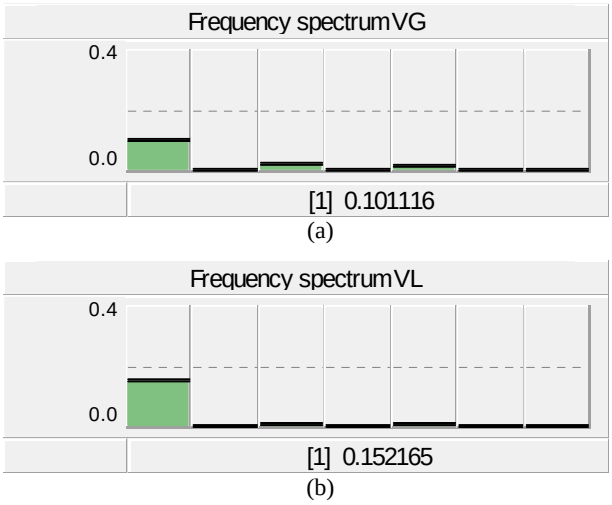

Fig.12 The frequency spectrums: (a) the grid voltage, (b) the load voltage.

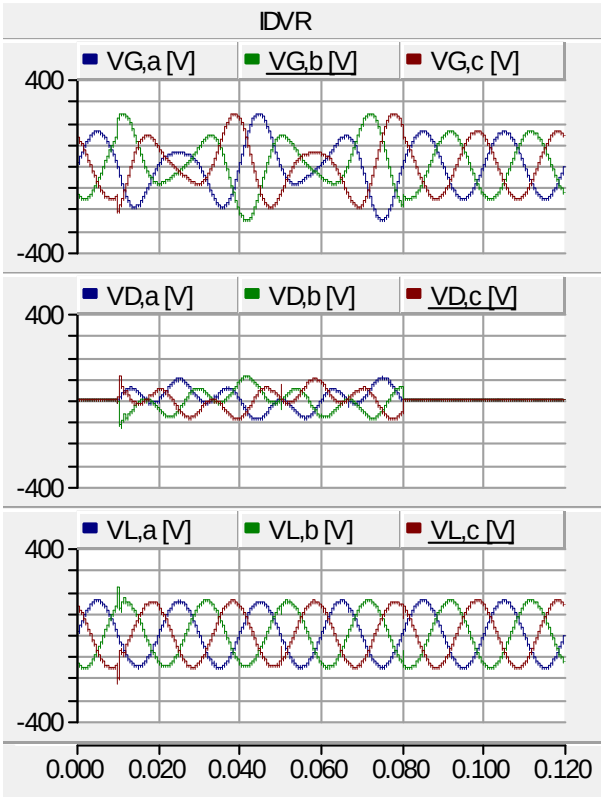

Fig. 13 Simulation results for the voltage flicker.

The compensation voltage under the flicker condition is shown in Fig. 13. In this figure, the voltage is in the normal condition in time interval between 0 and 0.01 sec. Then the voltage amplitude oscillates between 0.8 and 1.4 pu and the oscillation frequency is 30 Hz. Flicker is occurred between 0.01 and 0.08 sec. time interval. As the disturbance happens, IDVR starts to compensate through fast disturbance detection. As

presented in the figure, the load voltage is in the normal condition all the time.

The simulation results in case of the complete loss of voltage are presented in Fig. 14. As shown in the figure, in the first half-period, the grid voltage is in the normal condition. In the time interval between 0.01 and 0.08 sec., power outage occurs and simultaneously, IDVR starts to compensate the voltage. Since the injected voltage amplitude is great, the transient state is more evident in this case. There is no restriction for the compensation time interval because the required energy for compensation is directly provided by the other grid. As acclaimed features, the proposed IDVR is able to compensate severe voltage sags. Moreover, the proposed topology can be used as the uninterruptible power supply (UPS). Since the proposed topology has no need to the energy storage elements, the IDVR is superior in comparison with UPS.

Fig. 15 shows the voltage compensation under the unbalanced disturbance condition. The grid voltage is in the normal condition within the first half-period. Between 0.01 and 0.08 sec. the unbalanced voltage occurs. In this condition, the voltage amplitudes of a, b and c phases are 0.966, 0.26 and 0.71 pu and the phase angles of a, b and c phases are 15, -165 and -165 degrees, respectively. As acclaimed features, the proposed topology is able to compensate disturbances under unbalanced conditions.

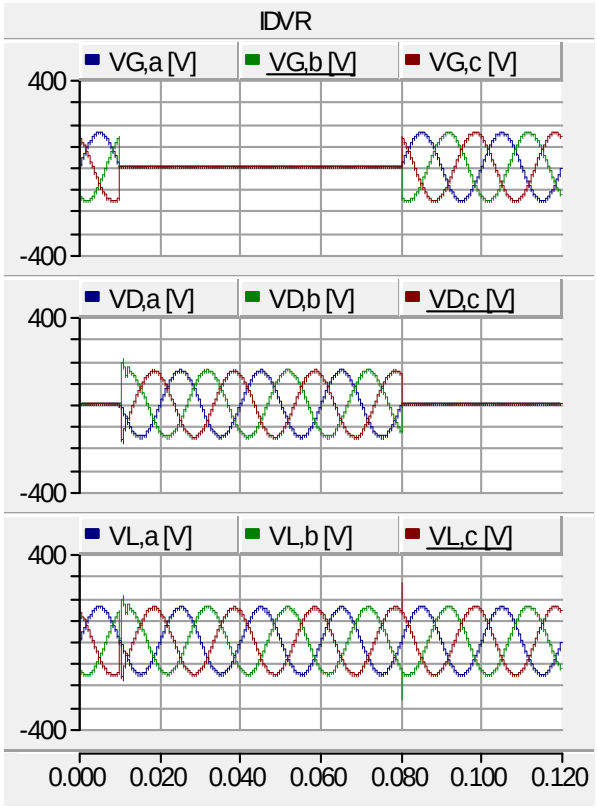

Fig. 14 Simulation results for the power outage condition.

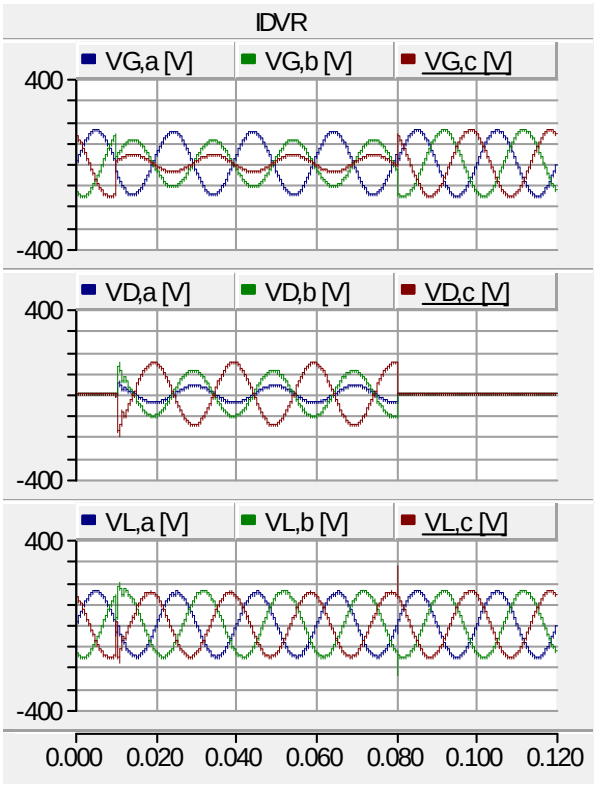

Fig. 15 Simulation results under the unbalanced disturbance condition.

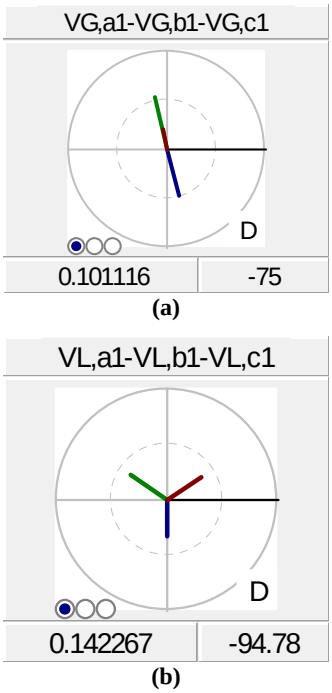

Fig. 16 Phasor diagrams: **(a)** grid voltages, **(b)** load voltages

The phasor diagrams of the grid voltages and the load voltage have been shown in Fig. 16. According to the figure, the grid voltage is under unbalanced

condition. Line faults and unbalanced loads are the main occurrence factors of asymmetric voltage in the grid. The unbalanced disturbance affects on proper performance of electrical components, such as: transformers and induction machines. Therefore, the necessary measures should be considered against any kind of disturbance, especially for asymmetric voltage condition. As shown in the figure the load voltage is compensated properly due to the presence of proposed topology. As a result, the proposed topology can be an appropriate option to protect the sensitive loads

5 Conclusion

In this paper, a new topology for IDVR with a fictitious dc-link is proposed. Due to lack of large capacitors and energy storage elements, the proposed topology has less cost, weight and volume in comparison with the conventional topology of IDVR. Moreover, the proposed topology is able to compensate the voltage under severe disturbance conditions and for any time duration due to the direct connection of converters to the grids. Unlike the presented conventional topologies for DVR and IDVR, the proposed topology is able to compensate the power outage which makes it to be a good alternative to UPS systems. Despite the conventional topology of ac/ac converters, the unidirectional switches are used instead of the bidirectional switches.

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