An Ultra High CMRR Low Voltage Low Power Fully Differential Current Operational Amplifier (COA)

A. Roohavar* and S. J. Azhari*(C.A.)

Abstract: this paper presents a novel Fully Differential (FD) ultra high Common Mode Rejection Ratio (CMRR) Current Operational Amplifier (COA) with very low input impedance. Its FD structure that attenuates common mode signals over all stages grants ultra high CMRR and Power Supply Rejection Ratio (PSRR) that makes it suitable for mixed mode and accurate applications. Its performance is verified by HSPICE simulations using TSMC 0.18 μm CMOS technology and ±0.75 V supply voltage that indicate such outstanding results of 81.1 dB gain, 298 MHz gain-bandwidth product, 64º phase margin, 28.2 mΩ input impedance, 159 dB CMRR and PSRR+/PSRR- of 174 dB/163 dB all at low power consumption of 0.302 mW. To study the robustness of the COA against technology and get such results close to measurement, Monte Carlo analysis is applied on both pre-layout and post layout simulations of the design. The results are as; 73.29 dB and 2.07 MHz, 1.92 Ω, and150.35 dB for A_i magnitude and bandwidth, R_i, and CMRR, respectively, in pre-layout case while change to; 66.58 dB and 1.44 MHz, 11.07 Ω, and 147.10 dB, for the same arrange, in post layout case. These measurement-like results thus, prove excellent practical performance of the proposed COA.

Keywords: Current Mode, High CMRR COA, Low Voltage.

1 Introduction

In recent years, the needs of low-voltage low power design of analog integrated circuits have gained increasing attention [1-4]. The main reasons are down-scaling of CMOS technology into submicron, increasing number of electronic devices on a single chip, world energy problems, serious environmental issues, expanding battery life in either portable or biomedical body implanted appliances such as mobile phone, hearing aid, etc. Under such restrictions, current-mode signal processing emerges as a promising solution since it can operate with a supply voltage of few hundred milli-volts larger than the threshold voltage of a MOS transistor [5]. Current signal swing is not limited by supply voltage hence current mode circuits can work effectively under reduced supply voltages [6-7]. Other potential advantages of current mode signal processing such as wider bandwidth, simpler circuitry, wider dynamic range and the likes have led to rapid implementation and development of such current-mode active elements as current conveyor, Current Differencing Buffered Amplifier (CDBA), Current Buffer (CB) and COA [8-18].

COAs are found in two main structures:1) Single input differential output structure which is the adjoint block of conventional differential input single output VOA and 2) FD structure (differential input differential output) which is the adjoint block of conventional differential input differential output VOA [17]. Fully differential structure offers many advantages over the single input differential output one. It provides inherent immunity to common mode signals, clock feed through, interferences and other types of common mode disturbances, wider dynamic range and the like [19]. It also has further flexibility and can be employed as a single input differential output COA if needed. A FD COA has to fulfill such requirements as very low input impedance, high common mode rejection ratio (CMRR), high power supply rejection ratio (PSRR), high current gain and high frequency response. Low voltage and low power consumption are also strongly demanded due to above mentioned reasons.

Although there are some fully differential COAs reported in literature [14-18], unfavorably none of those have shown the required performance. For example the COAs of [14-15], and [18] have high power consumption. Furthermore the COA of [16] has high supply voltage and poor CMRR. The large voltage COA

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of [16] has rather high input impedance. The COA of [17] owns the low f_T of 28 MHz.

In this paper we present a novel low voltage low power FD COA which exhibits very low input impedance, ultra high CMRR and PSRR. Thanks to the fully differential current buffer have been reported in [20] that provides the proposed COA with very low input impedance despite adopted low bias current. Meanwhile its very simple structure brings up a high unity gain bandwidth and low power consumption. Moreover FD structure and attenuating common mode signals at the input, gain and output stages results in the highest yet reported CMRR and strong immunity against supply voltage noises and disturbances. The organization of this paper is as follows: In section 2, the proposed FD COA is presented. Section 3 includes the simulation results of the proposed COA. Finally section 4 concludes the paper.

2 The Proposed COA Structure and Performance

A general fully differential COA is composed of three main blocks: input stage (current buffer), high current gain stage and output stage. In [14-16] input stage is class A type. Although class A input stage, enjoys simple structure, but it suffers from large consumed power and low dynamic range. Whereas class AB type input stage is more beneficial as input stage of COA since its input current can be several times larger than the bias current of transistors while consumes very low power. The conventional class AB input stage is shown in Fig. 1. It is composed of input transistors M1-M2 which are biased with Mb1-Mb2 and current sources IB1. Input currents are transferred to the output node by the pair of current mirrors of M3-M4 transistors and M5-M6 ones. The class AB input stage of Fig. 2 can handle currents several times larger than its bias current which is low enough to guarantee low consumed power. Unfavorably, it has high input impedance which makes it unsuitable for current mode circuits and high frequency applications. Its input impedance is given by Eq. (1) that can be very large especially for low bias currents of class AB.

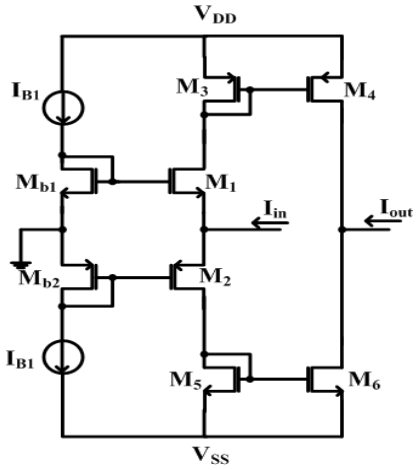

Fig. 1 The conventional class AB input stage.

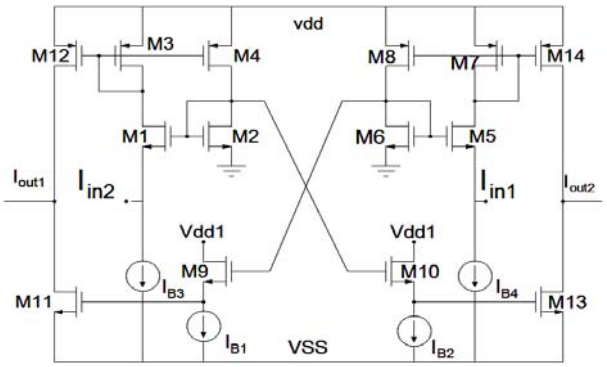

Fig. 2 The fully differential current buffer [20].

$$R_{in} = (g_{m1} + g_{m2})^{-1} \quad (2)$$

where g_{mi} is the transconductance of the related transistor.

Favorably input impedance of Fig. 1 can be greatly reduced by employing a source grounded transistors M_2 and M6 as is shown in Fig. 2 [20].

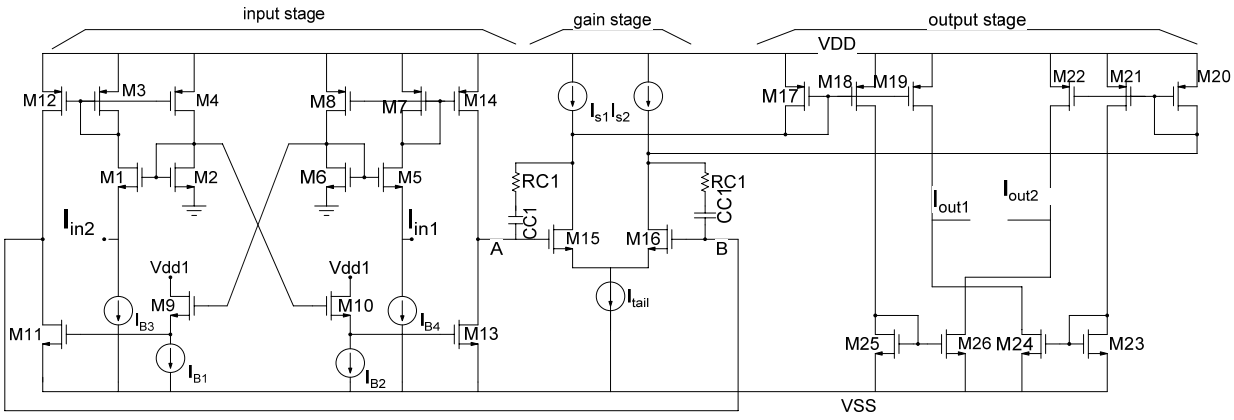

Fig. 3 Complete schematic of the proposed COA.

The input transistors of the current buffer; M_1 and M_5 are connected to source grounded transistors M_2 and M_6. Thus the inputs of the current buffer become virtually grounded which means an ideally zero input impedance resulting in very low input impedance given by:

$$R_{in}=\frac{1}{g_{m1,5}}-\frac{1}{g_{m2,6}} \quad (3)$$

where $g_{m1,5}$ and $g_{m2,6}$ are mutual transconductance of related transistors and can be maintained as much to satisfy the required input impedance.

The complete schematic of the proposed COA including input stage, gain stage, output stage and compensation network is shown in Fig. 3. The output currents of input stage are converted to voltage at nodes A and B and then are converted back to current by gain stage which is a differential amplifier composed of transistors M15-M16 and a high output impedance tail current source of I_{tail}. As an excellent plan, the high output impedance current source proposed in [22] and shown in Fig. 4, is used at the gain stage in order to both attenuate common mode signals and widen the dynamic range of the COA which both are mandatory for high CMRR feature. The gain stage should have large bias current to provide high current gain. Such a high bias current directly enters to the output stage and results in a significant increase in the total power consumption. To avoid, the technique used in [23] is deliberately modified in the gain stage. This is another brilliant arrangement to save the power in the proposed COA. Deliberately, I_{S1} and I_{S2} which are some fraction of $I_{tail}/2$ absorb some portion of bias current of gain stage and reduce the bias current of output stage. Therefore bias current of gain stage can be set to an arbitrary value to provide the required gain meanwhile total power consumption can be simply reduced by reducing bias current of output stage. The output current of gain stage is transferred to the output node by simple current mirrors composed of transistors M17-M26 as is shown in Fig. 3. To make the output stage a deserving partner in increasing the CMRR of the proposed COA, another effective technique is devised.

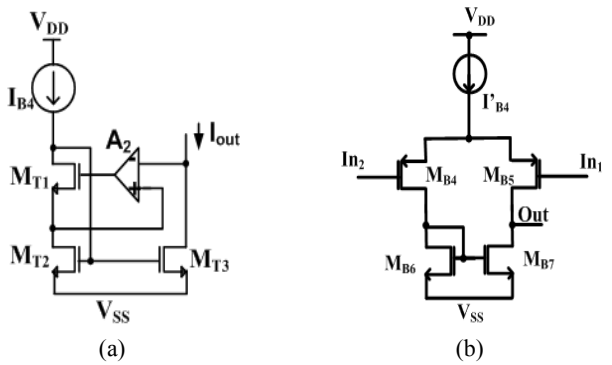

Fig. 4 (a) the used high output impedance tail current source [22] (b) Implementation of the used auxiliary amplifier of A2.

That is cross coupled connection of the PMOS and NMOS current mirrors joining to so many excellent plans used to remarkably enhance the performance of the proposed COA. Thanks to this last plan of cross coupled connection that is such arranged to cancel the remained common mode signals at the output node by subtracting them from each other meanwhile introduces an intrinsic amplification of two for differential signals. This elaborately composed structure grants the overall COA a very high CMRR. Frequency compensation of the overall COA can be done by inserting miller capacitors and nullifying resistors between nodes A-A' and B-B' as is shown in Fig. 3. The overall small signal gain and CMRR of the proposed COA is found as:

$$A_{id}=\frac{i_{od}}{i_{id}}=(\lambda_1+\lambda_2.\alpha.\frac{g_{m11,13}}{g_{m2,6}}) \times[r_{o14}\|r_{o13}]\times gm_{15}\times(\lambda_3+\lambda_3\times\lambda_4) \quad (4)$$

$$A_{ic}=\frac{i_{oc}}{i_{ic}}=(\lambda_1-\lambda_2.\alpha.\frac{g_{m11,13}}{g_{m2,6}}) \times\frac{[r_{o14}\|r_{o13}]\times gm_{15}\times(\lambda_3-\lambda_3\times\lambda_4)}{(1+2\times gm_{15}\times R_{SS})} \quad (5)$$

$$CMRR=\frac{A_{id}}{A_{ic}}=\frac{(\lambda_1+\lambda_2.\alpha.\frac{g_{m11,13}}{g_{m2,6}})}{(\lambda_1-\lambda_2.\alpha.\frac{g_{m11,13}}{g_{m2,6}})} \times(1+2\times gm_{15}\times R_{SS})\times\frac{(\lambda_3+\lambda_3\times\lambda_4)}{(\lambda_3-\lambda_3\times\lambda_4)} \quad (6)$$

where λ1 and λ2 are the current gain of M3, M12 and M7, M8 current mirrors respectively. RSS is the output impedance of IB4 current source, λ3 and λ4 are the current gain of M17-M19 and M25-M26 current mirrors respectively.

3 COA Simulation Results

The proposed fully differential COA of Fig. 3 is designed using 0.18 μm TSMC CMOS technology parameters and simulated with HSPICE utilizing supply voltage of ±0.75 V. To achieve the best overall values for most important parameters of the proposed COA, the aspect ratios of transistors are selected as are given in Table 1 regarding the performance relations of (1)-(6).

Table 1 Transistors aspect ratios.

Transistor	Aspect Ratio (μm/μm)	Transistor	Aspect Ratio (μm/μm)
M1, M5	21.5/0.8	M17,M20	1/1
M2, M6	4/0.5	M18,M21	18/0.5
M3, M7	20/0.5	M19,M22	56/0.3
M4, M8	11/0.5	M23,M25	1/3
M9, M10	1/1.5	M24,M26	2/1
M11, M13	1/1	MB4 - MB7	10/0.8
M12, M14	3.9/0.5	MT1	100/0.5
M15, M16	2/0.5	MT2	10/0.5
		MT3	80/0.5

The selected element values and bias currents are as: $I_{B1}=I_{B4}=20$ µA, $I_{B2}=I_{B3}=6$ µA, $I_{S1}=I_{S2}=4$ µA, $R_{c1}=0.3$ kΩ, $C_{c1}=0.02$ pF. Real current sources are implemented as simple current mirrors and the value of R_L is selected as 1 kΩ.

The A_{id} frequency performance of the proposed COA is shown in Fig. 5 with an open loop gain of 81.1 dB. Its unity gain frequency is found to be 298 MHz, at which the phase margin is 64º (-116º). The CMRR and PSRR behaviors of the proposed COA are illustrated in Fig. 6. It shows a CMRR of 159 dB that reaches to zero dB at high frequency of 552 MHz. Moreover due to its fully differential nature, the proposed COA has high Power Supply Rejection Ratio (PSRR) as is also shown in Fig. 6.

The simulated positive and negative PSRR are 174 dB and 163 dB respectively which shows the high ability of the proposed COA in rejecting supply noises and makes the proposed COA an excellent candidate for mixed mode applications. To investigate the robustness of the proposed COA against process non-idealities and to obtain such results close to measurement as is generally believed, pre-layout and post layout both with Monte Carlo simulations are performed. Monte Carlo simulations are carried out by considering Gaussian distributed 2% mismatches on related parameters of all transistors in 30 runs with 3σ standard deviation. The results of pre-layout cases (plus Monte Carlo) are shown in Figures 7-10 for CMRR, A_i magnitude and bandwidth, and R_i as; 150.36 dB, 73.29 dB and 2.607 MHz, and 1.92 Ω, respectively. These results for post layout cases (plus Monte Carlo) are verified as; 147.10 dB, 66.58 dB and 1.44 MHz, and 11.07 Ω by figures 11-14 with the same order. Monte Carlo simulation results prove well robust performance of the proposed COA against mismatches.

The simulation results show that the proposed COA consumes the total power (P_d) of 302 µW at pre-layout (311 µW at post layout). Fig. 15 shows the layout of the proposed amplifier with dimensions of (35 µm×58 µm).

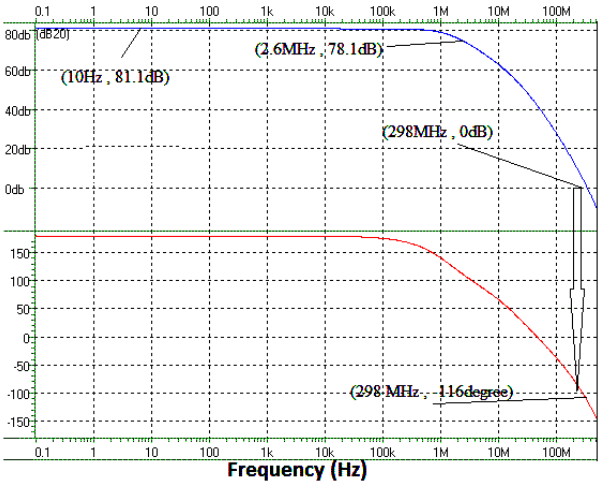

Fig. 5 A_i magnitude and phase frequency performance.

To reduce the cross chip gradients towards the performance improvement of the differential pairs the layout of that part is performed using common-centroids technique. Important parameters of the proposed COA (all types of; simulation, pre-layout plus Monte Carlo and post layout plus Monte Carlo) are compared with those (only simulations) of some other so far reported fully differential COAs in Table 2. For a fair comparison the figure of merit (FOM) defined as (6) is also included in Table 2. Favorably, it proves the distinguished superiority of the proposed COA over all others (larger than others from 93 dB to 276 dB).

$$FOM = \frac{R_{out}(\Omega)\times Ai\times CMRR\times f_T(MHz)}{V_{DD}(V)\times R_{in}(\Omega)\times P_d(mW)} \qquad (7)$$

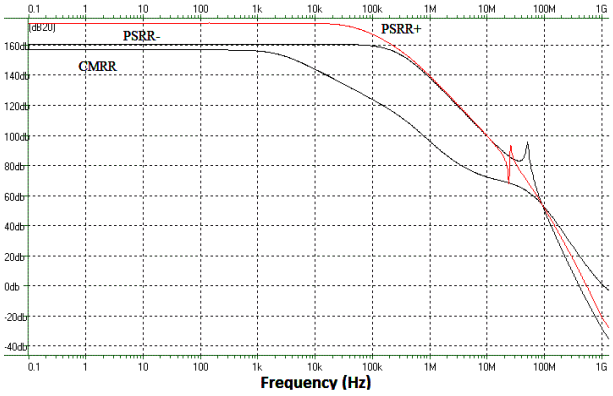

Fig. 6 CMRR and PSRR frequency performance.

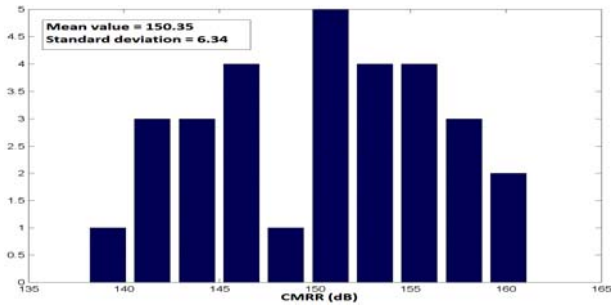

Fig. 7 Statistical distribution of CMRR (dB) in presence of mismatches.

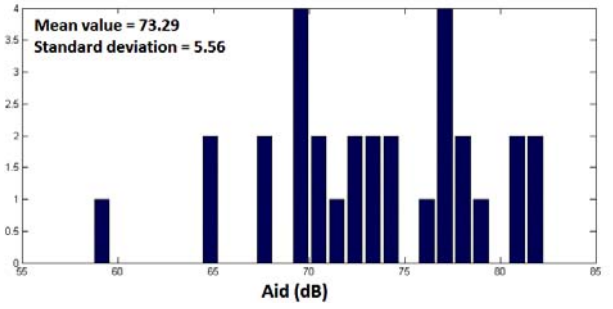

Fig. 8 Statistical distribution of A_{id} (dB) in presence of mismatches.

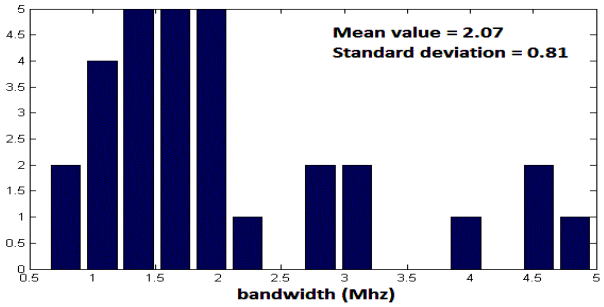

Fig. 9 Statistical distribution of f_{-3dB} in presence of mismatches

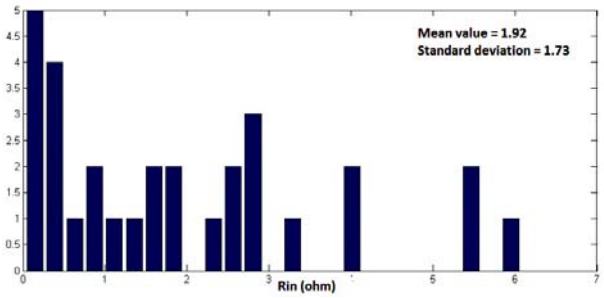

Fig. 10 Statistical distribution of R_{in} in presence of mismatches.

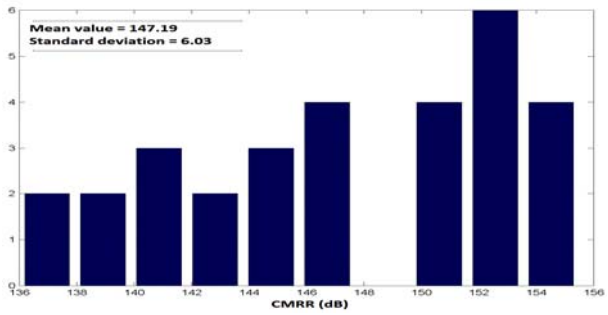

Fig. 11 Statistical distribution of CMRR in presence of mismatches after post layout.

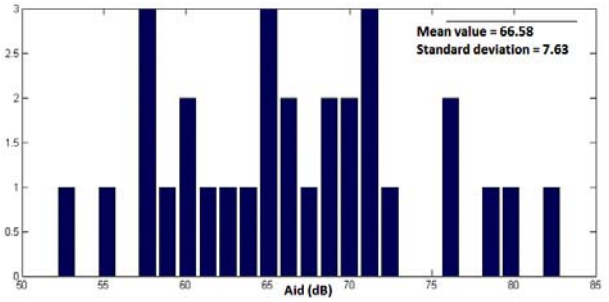

Fig. 12 Statistical distribution of A_{id} in presence of mismatches after post layout.

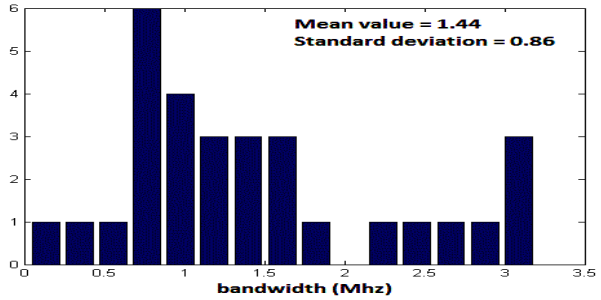

Fig. 13 Statistical distribution of f_{-3dB} in presence of mismatches after post layout.

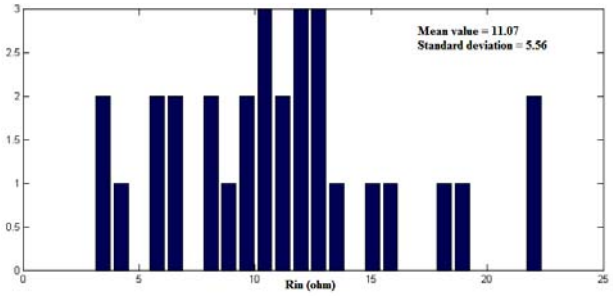

Fig. 14 Statistical distribution of R_{in} in presence of mismatches after post layout.

Table 2 Comparison between the proposed COA and other related works.

Performance Specifications	R_i (Ω)	R_o (MΩ)	A_i		Phase margin Degree	f_T MHz	CMRR (dB)	Sup (V)	P_d (mW)	FOM (dB)	Technology CMOS (µm)	Type of Results
			Value (dB)	f_{-3dB} MHz								
[14]	28	7.8	72	.07	52	28	127	2.5	0.675	460	0.25	Post-Layout
[16]	120	30	96	NA	60	90	NA	3	0.66	417	0.35	Simulation
[18]	123	14	107	NA	62	102	113	3	1.15	530	0.35	Simulation
[24]	NA	NA	70	$100H^0$	NA	NA	105	0.6	0.01	NA	0.18	Simulation
[25]	13	89	93	8.2	89	276	137	1.5	1.37	174	0.18	Pre-L* + MC[a]
	22	33	88	6.9	131	247	96	1.5	1.43	155	0.18	Pre-L* + MC[a]
Proposed Work	.028	0.105	81.1	2.67	64	298	159	1.5	0.302	623	0.18	Simulation
	1.92	.105	73.29	2.07	64	276	150.35	1.5	0.302	560	0.18	Pre-Layout + Monte Carlo
	11.07	.111	66.58	1.44	72.8	247	147.19	1.5	0.311	532	0.18	Post-Layout + Monte Carlo

*=Layout, [a]=Monte Carlo, °=Hertz

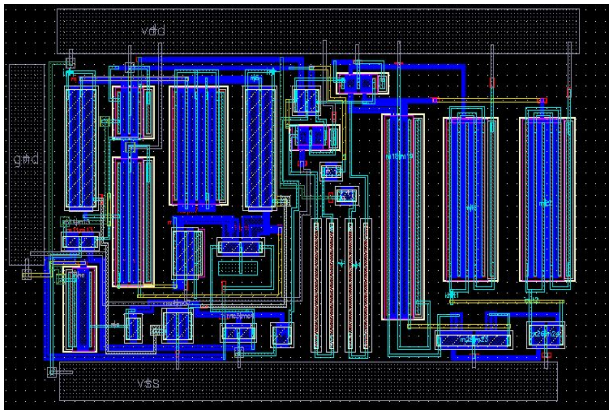

Fig. 15 COA Layout.

4 Conclusion

In this work, a novel FD high CMRR COA with very low input impedance and high frequency operation is proposed and full simulation types of results included pre-layout, post layout and Monte Carlo are performed. Due to deliberate design yet the simple circuitry of the proposed COA, higher than 81.1 dB current gain and ultra-high CMRR of 159 dB are obtained with only 302 µw power supply. It also offers very low input impedance and very high FOM.

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