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EKV Model Based Analog/RF CMOS Design Pre-SPICE Tool

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Abstract: A novel simplified EKV model base analog/RF CMOS design pre-SPICE tool is presented in this paper. Addition to facilitating the sizing process, this CAD tool can also optimize circuit characteristics. By having a web address, users can access it without installing any software. Using a graphical and a numerical view, the designer can select degrees of freedom and observe the MOS circuit performance. Through the use of charts versus IC, the graphical view can show tradeoffs in circuit performance in real-time. Charts can be displayed simultaneously in both linear and logarithmic scales. IC_{CRIT}, is also available and can be displayed on the charts. This tool is not limited to one process and it is possible to select different processes. It is efficient for pre-SPICE designs, enhancing intuitive understanding and the designer's experience for future projects while eliminating the need for trial-and-error simulations. Furthermore, the predicted results align well with simulation outcomes, demonstrating the effectiveness of the design and optimization method presented. Two methodologies for selecting optimum ICs are presented by this tool. These are illustrated by the study of linearity indices, AIP3 and IIP3, in one-stage and two-stage differential amplifiers and the design of a single-ended OTA.

Keywords: Enz Krummenacher Vittoz, Radio Frequency, Simulation Program with Integrated Circuit Emphasis, Computer-aided design, Inversion Coefficient, Critical inversion coefficient. Operational Transconductance Amplifier.

1 Introduction

THE design and control of analog/RF circuits to achieve the predefined characteristics of an application due to the multi-parameter design space, is always one of the basic challenges of designers [1]. Nowadays, by inherent reduction of the power supply voltage, the development of low power and low-cost analog/RF circuits has become more significant [2,3,4,5]. On the other hand, the complex and time-consuming design process, has motivated researchers to provide automatic CAD tools [6]. Finally, in addition to the possibility of selection of tradeoffs and optimization, this tool should perform all of the aforementioned steps automatically as much as possible [7]. One of the primary issues of the design methodology is the selection of the appropriate device model. Device models can be broadly classified into the following distinct categories [8]:

physical these models would often consist of coupled nonlinear partial differential equations to accurately describe the physical effects in the device.

Empirical these models consist of curve fitting with no physical significance attached to the equations.

Semi-empirical Such models are physics based, with suitable assumptions and approximations to keep the model equations reasonably simple for hand calculations [9,10]. So, semi-empirical models are suitable for pre-SPICE methodologies. An example of these models is the EKV model of the MOS device.

In 1995, C. Enz, F. Krummenacher and E.A. Vittoz developed the EKV model for MOS devices that

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describe transistor behavior continuously from weak to strong inversion through the IC [11,12]. The IC is a normalization of the drain current, I_D, to the specific current, I_{spec}, which consists of the technological parameters and the geometry of the transistor,

$$IC = \frac{I_D}{I_{spec}} = \frac{I_D}{I_0\left(\frac{W}{L}\right)}\ , \tag{1-a}$$

$$I_0 = 2n\mu C_{OX}{U_T}^2 \tag{1-b}$$

where L and W are the gate length and width, n is the slope factor, μ is the constant low-field mobility, C_{OX} is the oxide capacitance per unit area and $U_T = \mathrm{kT/q} = 26\ \mathrm{mV}$ is the thermodynamic voltage at standard room temperature. The value of the IC indicates the level of inversion of a transistor, regardless of the technology or the size of this transistor:

- IC < 0.1, Weak Inversion (WI),
- 0.1 <IC < 10, Moderate Inversion (MI),
- IC > 10, Strong Inversion (SI),

In recent years, as MOS devices' channel length has shrunk and their operating points have shifted to WI and MI regions, V_{EFF} has become less relevant for analog/RF circuit designers as a key design parameter [13,14]. The drain current of a MOS transistor in 28 nm FDSOI is plotted against the gate-source voltage (V_{GS}) in Fig. 1a and against IC in Fig. 1b [15]. Fig. 1a indicates that the SI region spans a wide voltage range but covers only one decade of current, while the WI and MI regions cover multiple decades from 0 to 0.5 mV. In contrast, Fig. 1b shows that one decade of current corresponds to one decade of IC, due to their linear relationship. Thus, IC is more suitable for modeling MOS devices in the WI and MI regions than V_{GS}. Additionally, key parameters of the MOS transistor, such as intrinsic bandwidth, gain, and transconductance efficiency, can be analyzed using IC [16]. This allows for determining appropriate operating points for transistors in a circuit by adjusting the inversion coefficients of MOS devices. If the IC is used instead of V_{EFF} as a design variable, then the MOS transistor parameters such as g_m, g_m/I_D and f_T all give straight lines on log–log scales [17].

Several IC-based Pre-SPICE tools have been developed for the design of analog/RF circuits, which, in addition to providing design intuition, avoid iterative and tedious trial and error simulations by complex models. In 1996, the first sizing tool, actually called Analog Designer, created by Christian Enz [18]. It allows calculation of important design parameters of the single transistor from the basic inversion coefficient. It is limited to a single transistor and does not display all of the parameters related to MOS devices. Another CAD tool, developed by D.M. Binkley, provides design guidance as the designer explores drain current, inversion coefficient and channel length [19]. Despite the calculation of almost all parameters of the MOS device, it lacks a graphical representation in the form of charts versus IC. In 2007, this tool has been replaced by the analog CMOS design, tradeoffs and optimization spreadsheet. In another CAD tool that is implemented using ADS software, the optimization has been done specifically for different amplifier circuits [20]. This method is limited to the model provided by the specific foundry. In another work, a tool using MATLAB software is proposed to measure the geometry of MOS devices of a circuit using optimizing the inversion coefficient [21].

In this paper, a new CAD tool based on the simplified EKV model is introduced, which finally determines the optimal values of the characteristics of the MOS devices by a new design method. This tool, which actually called Analog/RF CMOS Design Pre-SPICE Tool and can be used on all web browser softwares, is implemented in the style of server and client with JavaScript language. Users can access it without installing any software just by having a web address. Design interface of the tool has two sections of numerical data and graphical analysis. these sections provide both numerical report view of MOS performance and charts view versus IC dynamically. In the EKV model equations used to calculate the parameters and characteristics of circuit devices, small geometry effects are also considered. Charts can be displayed simultaneously in both linear and logarithmic scales. IC_{CRIT}, which denotes the transition point between SI transconductance efficiency without small geometry effects and the velocity saturated value, is also available and can be displayed on the charts by red color. This tool is not limited to one process and it is possible to select different processes.

2 EKV Model Base Analog/RF CMOS Design Pre–SPICE Tool

Fig.2 shows the architecture for Analog/RF CMOS Design Pre–SPICE Tool which includes a numerical data view, a graphical analysis view, a circuit analysis view and a CSV format reporting view design interface. As illustrated in Fig.3, that shows a real view of mentioned tool, it is possible to select MOS devices by desired CMOS processes from 0.18μm to 22nm in the numerical data section. If the process intended by the designer is not available in the default processes, the designer can easily add this possibility by completing a simple default text file. The possibility of designing RF circuits are also included in this tool by selecting passive elements such as resistors, inductors and capacitors. In the following, these sections are discussed in detail:

2.1 Numerical Data

The numerical data section consists of four parts: process parameters, degrees of freedom, primary

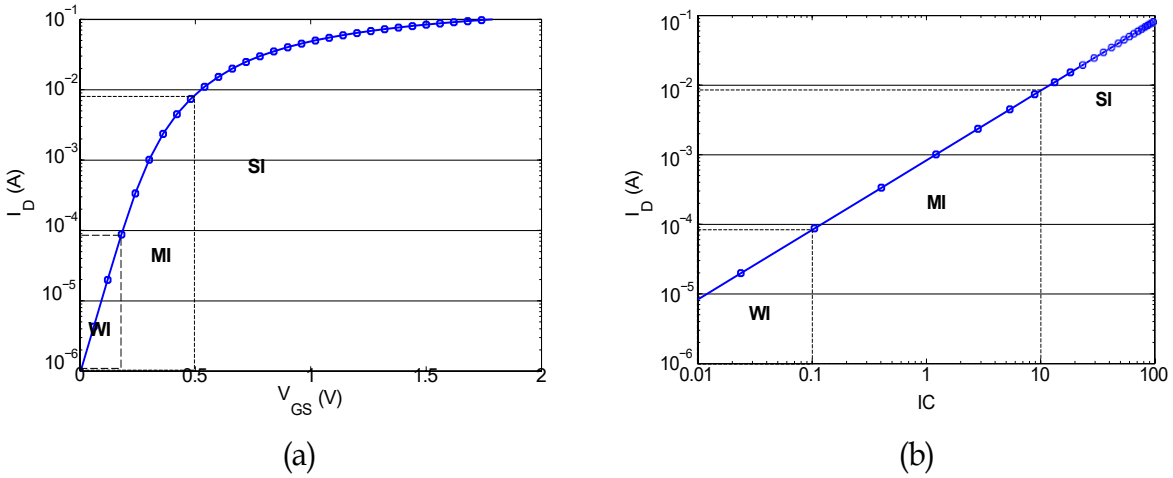

Fig 1. (a) I_D versus V_{GS} and (b) I_D versus IC for a transistor with a gate width of 50µm in 28 nm FDSOI [15].

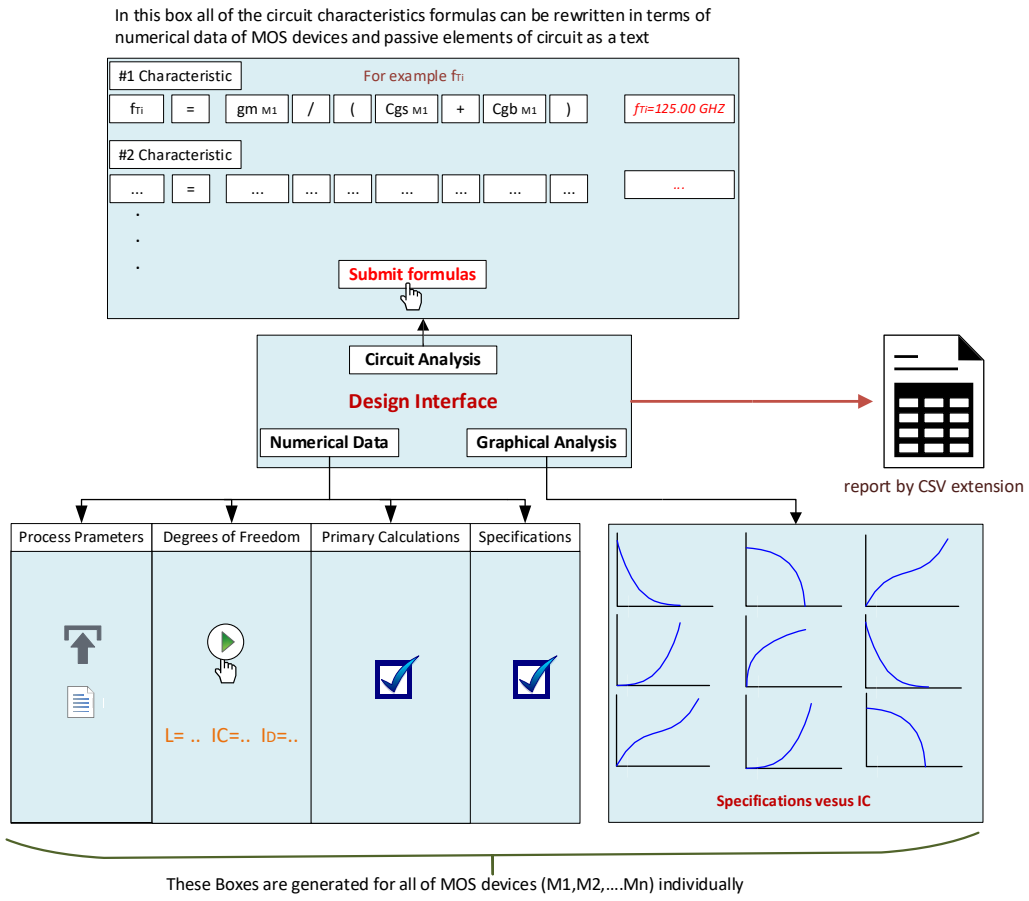

Fig 2. Architecture of analog/RF CMOS design Pre SPICE tool.

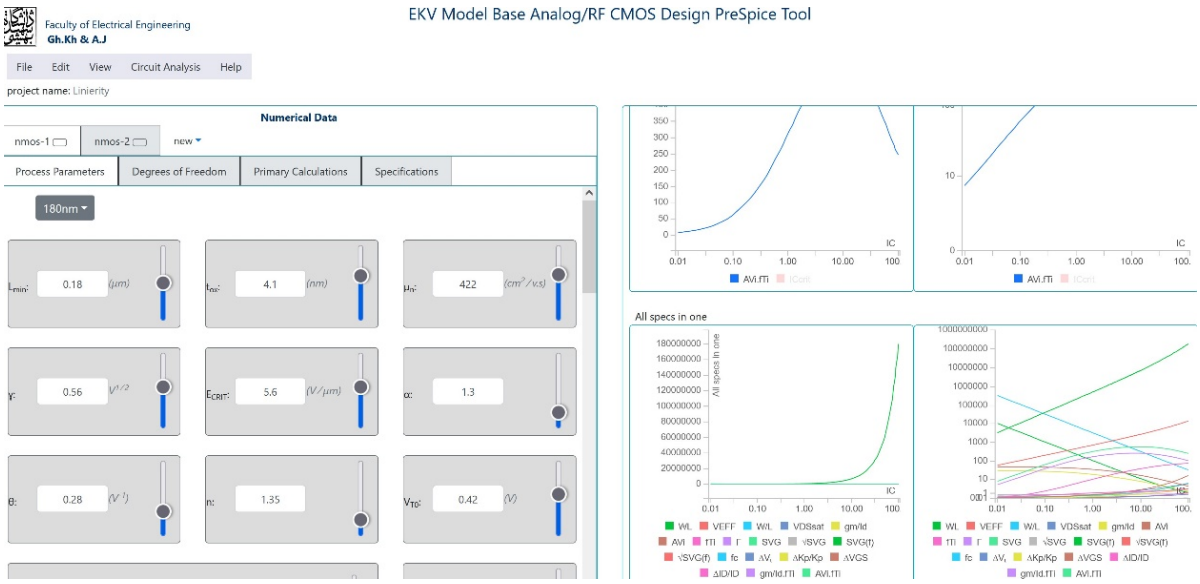

Fig 3. Design interface of EKV model base Analog/RF CMOS Design Pre–SPICE Tool.

calculations and specifications. In this section, all of the devices of analog/RF circuit are selected and the designer based on default characteristics of a circuit and using degrees of design freedom, determine bias and sizing of transistors. In the following, these parts are discussed in detail:

2.1.1 Process Parameters

Although the number of process parameters and equations of the EKV model is less than compact BSIM model, but nearly 70 parameters are needed for the description of MOS device and its effects [22]. One of the methods for extracting the parameters of EKV model is converting the BSIM model parameters to EKV, which has been done using the Levenberg-Marquardt algorithm for 0.18µm CMOS process [23]. In this paper, only 26 parameters have been used to develop the process parameters, whose along with 5 optional parameters are listed in Table 1. Other parameters are automatically extracted using simple equations in the primary calculations part. In fact, the simplified EKV model has been used in Analog/RF CMOS Design Pre–SPICE Tool.

2.1.2 Degrees of Freedom

As illustrated in Fig.4, in the degrees of freedom menu, it is possible to choose 6 parameters, I_D, IC, L, g_m/I_D, V_{EFF} and W. By choosing IC as a main design parameter, g_m/I_D and V_{EFF} directly are given by [7]:

$$V_{EFF} = 2nU_T\, ln\left(e^{\sqrt{A}} - 1\right) \qquad (2-a)$$

$$A = IC\left[1 + \left(\frac{IC}{4IC_{CRIT}}\right)^{\beta}\right]^{\frac{1}{\beta}} \qquad (2-b)$$

$$IC_{CRIT} = \left[\frac{\left(LE_{CRIT} \parallel \frac{1}{\theta}\right)}{4nU_T}\right]^2 \qquad (2-c)$$

$$\left(LE_{CRIT} \parallel \frac{1}{\theta}\right) = \frac{LE_{CRIT} * \frac{1}{\theta}}{LE_{CRIT} + \frac{1}{\theta}} \qquad (2-d)$$

$$\frac{g_m}{I_D} = \frac{1}{nU_T\left(\sqrt{B + 0.25} + 0.5\right)} \qquad (3-a)$$

$$B = IC\left(1 + \frac{IC}{IC_{CRIT}}\right) \qquad (3-b)$$

where V_{EFF} is effective gate-source voltage, A and B are replacement parameters of IC in V_{EFF} and g_m/I_D relationships respectively that include small geometry effects, β is Exponent for add small geometry effects (SGE) in V_{EFF}, IC_{CRIT} = 31.83 is the critical IC (Fig. 5), E_{CRIT} is velocity saturation critical horizontal electric field, θ is vertical field mobility reduction factor and g_m/I_D is transconductance efficiency. By known I_D, channel width is given by [5]:

$$W = \left(\frac{L}{IC}\right).\left(\frac{I_D}{I_0}\right) \qquad (4)$$

2.1.3 Primary Calculations

In this part, 38 different parameters, including constants, voltages, capacitors, etc., which are listed in Table 2, are automatically calculated using design parameters and degrees of freedom as the first step of calculations.

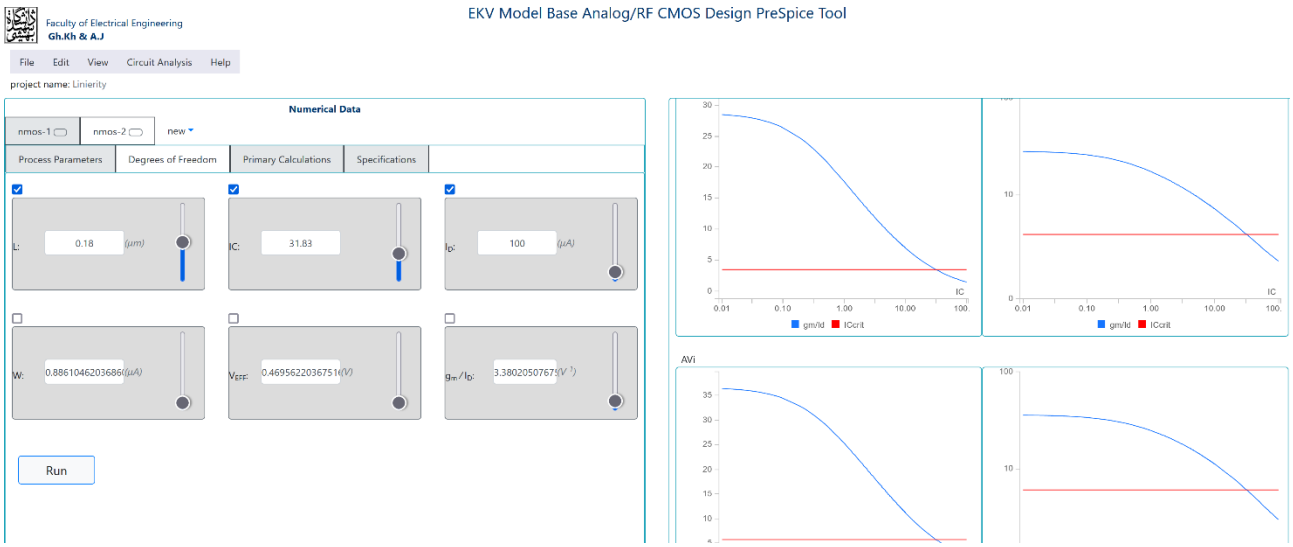

Fig 4. Design interface of EKV model base Analog/RF CMOS Design Pre–SPICE Tool

Table 1. Process parameters and their values for nMOS and pMOS transistors in the 0.18μm CMOS process.

Parameter	Description	Value for nMOS	Value for pMOS	Unit
t_{ox}	Oxide Thickness	4.1	4.1	nm
μ	Low Field Mobility	422	89.2	$\mu A/V^2$
Y	Body Effect Factor	0.56	0.61	$V^{1/2}$
V_{sat}	Saturation Velocity	90659.09	151306.8	m/s
E_{CRIT}	Critical Horizontal Electric Field	5.6	14	$V/\mu m$
α	Velocity Saturation Transition Exponent	1.3	1.3	--
n	Slope Factor	1.35	1.3	--
V_{T0}	Threshold Voltage	0.42	0.42	V
θ	Mobility Reduction Factor	0.28	0.35	V^{-1}
β	Exponent for Velocity Saturation and VFMR Effects	0.8	0.9	--
DVT_{DIBL}	Threshold Voltage Change Due to DIBL for Lmin	-8	10	mV/V
$DVT_{DIBLEXP}$	Exponent Describing Reduction in DVT_{DIBL}	3	3	--
DL	Lateral Diffusion at Length	0.028	0.051	μm
DW	Lateral Diffusion at Width	0	0	μm
V_{AL}	Early Voltage Factor	10	10	$V/\mu m$
K_{F0}	Flicker Noise Factor	3.18e-23	2.38e-31	C^2/cm^2
V_{KF}	Flicker Noise Factor Voltage	1	0.25	V
AF	Flicker Noise Slope	0.85	1.05	--
A_{VT0}	Threshold Voltage Mismatch Factor	5	5	mV. μm
A_{KP}	Transconductance Mismatch Factor	0.02	0.02	μm
$\widetilde{C_{gd1}}$	Normalized Gate-Drain Intrinsic Capacitance	0	0	--
C_{GSOV}	Gate-Source Overlap Capacitance	0.94	0.64	$fF/\mu m$
C_{GDOV}	Gate-Drain Overlap Capacitance	0.94	0.64	$fF/\mu m$
C_{GBOV}	Gate-Body Overlap Capacitance	0	0	$fF/\mu m$
ϕ_F	Half of Fermi Potential	0.425	0.425	V
L_{min}	Minimum Channel Length	0.18	0.18	μm
	Optional user design inputs			
f	Operation Frequency	--	--	HZ
V_{DD}	Supply Voltage	--	--	V
V_{SB}	Source-Body Voltage	--	--	V
V_{DS}	Drain-Source Voltage	--	--	V
T	Temperature	--	--	K

Table 2. Parameters of primary calculations part in analog/RF CMOS design Pre–SPICE tool.

Parameter	Description	Unit
$V_T = V_{T0} + (n-1)V_{SB}$	Threshold Voltage	V
$C_{OX} = \frac{34.5}{t_{ox}}$	Gate-Oxide Capacitance Per Area Unit	$fF/\mu m^2$
$U_T = 25.85(\frac{T}{300})$	Thermal Voltage	mV
$K = \mu C_{OX}$	Transconductance Factor	$\mu A/V^2$
$I_0 = 2n\mu C_{OX}{U_T}^2$	Technology Current	μA
$(LE_{CRIT})_{min}{}' = (LE_{CRIT}) \parallel \frac{1}{\theta}$	Minimum Equivalent Velocity Saturation Voltage	V
$L_{sat} = \frac{2\mu U_T}{V_{sat}}$	Velocity Saturation Length	μm
$\lambda_C = \frac{L_{sat}}{L}$	Velocity Saturation Coefficient	--
$C_{GOX} = WLC_{OX}$	Gate-Oxide Capacitance	fF
$X = \frac{(\sqrt{IC+0.25}+0.5)+1}{(\sqrt{IC+0.25}+0.5)^2}$	A Factor for Calculating Intrinsic Capacitances	--
$\Gamma = \frac{1}{1+IC}(\frac{1}{2}+\frac{2}{3}IC)$	Thermal Noise Factor	--
$\widehat{C_{gbi}} = (\frac{X+1}{3})(\frac{n-1}{n})$	Normalized Gate-Bulk Intrinsic Capacitance	--
$\widehat{C_{gsi}} = (\frac{2-X}{3})$	Normalized Gate-Source Intrinsic Capacitance	--
$(LE_{CRIT})' = (LE_{CRIT}) \parallel \frac{1}{\theta}$	Equivalent Velocity Saturation Voltage	V
$V_A(CLM) = V_{AL}L$	Early Voltage Due to Channel Length Modulation	V
$V_A(DIBL) = \frac{1}{g_m/I_D\left[-DVT_{DIBL}.\left(L_{min}/L\right)^{DVT_{DIBLEXP}}\right]}$	Early Voltage Due to Drain Induced Barrier Lowering	V
$IC_{CRIT_{min}} = [\frac{\left(L_{min}E_{CRIT} \parallel \frac{1}{\theta}\right)}{4nU_T}]^2$	Minimum Critical Inversion Coefficient	--
$IC_{CRIT} = [\frac{\left(LE_{CRIT} \parallel \frac{1}{\theta}\right)}{4nU_T}]^2$	Critical Inversion Coefficient	--
$A = IC\left[1+\left(\frac{IC}{4IC_{CRIT}}\right)^{\beta}\right]^{\frac{1}{\beta}}$	A Factor for Considering Velocity Saturation and VFMR Effects in VEFF	--
$B = IC(1+\frac{IC}{IC_{CRIT}})$	A Factor for Considering Velocity Saturation and VFMR Effects in gm/ID	--
$L_{eff} = L - 2DL$	Effective Length	μm
$W_{eff} = W - 2DW$	Effective Width	μm
$C_{gbi} = \widehat{C_{gbi}}.C_{GOX}$	Gate-Bulk Intrinsic Capacitance	fF
$C_{gsi} = \widehat{C_{gsi}}.C_{GOX}$	Gate-Source Intrinsic Capacitance	fF
$C_{gdi} = \widehat{C_{gdi}}.C_{GOX}$	Gate-Drain Intrinsic Capacitance	fF
$C_{GBO} = C_{GBOV}.W$	Gate-Bulk Extrinsic Capacitance	fF
$C_{GSO} = C_{GSOV}.W$	Gate-Source Extrinsic Capacitance	fF
$C_{GDO} = C_{GDOV}.W$	Gate-Drain Extrinsic Capacitance	fF
$C_{gb} = C_{gbi} + C_{GBO}$	Gate-Bulk Capacitance	fF
$C_{gs} = C_{gsi} + C_{GSO}$	Gate-Source Capacitance	fF
$C_{gd} = C_{gdi} + C_{GDO}$	Gate-Drain Capacitance	fF
$\eta = n - 1$	Body Effect Transconductance Ratio	--
$\varphi_0 = 2\varphi_F + 4U_T$	Built in Potential	V
$V_{GS} = V_{EFF} + V_T$	Gate-Source Voltage	V
$AV_T = AV_{T0}(1+\frac{V_{SB}}{2\varphi_0})$	Threshold Voltage Mismatch Factor	$mV.\mu m$
$K_F = K_{F0}(1+\frac{V_{EFF}}{V_{KF}})^2$	Flicker Noise Factor for All Regions	C^2/cm^2
$K_{GA} = \frac{80e^{-14t_{ox}}}{{t_{ox}}^2}$	Gate-Leakage Current Parameter1 for NMOS	$A/\mu m^2V^2$
$K_{GB} = 1.13t_{ox}$	Gate-Leakage Current Parameter2 for NMOS	V^{-1}

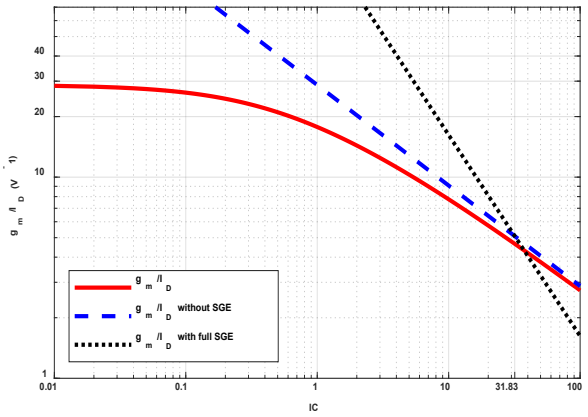

Fig 5. Transconductance efficiency versus inversion coefficient for an L = 0.18µm, nMOS device in a 0.18µm CMOS process.

2.1.4 Specifications

As shown in Fig.6, using process parameters, degrees of freedom and primary calculations, all the specifications of devices in circuit, including sizing relationships, DC bias parameters, small signal parameters, gain and bandwidth relationships, gate referred thermal and flicker noise parameters, local area DC mismatch parameters, gate-source leakage current and figure of merit factors for low power RF designs are automatically calculated using simple, accurate relationships. These specifications and their related relationships are listed in Table 3.

2.2 Graphical Analysis

The tradeoffs in circuit performance for a given drain current in saturation is demonstrated by the MOSFET operating plane given in Fig.7 [24,25]. As illustrated in the figure, MOS devices should be individually located at different locations on the operating plane considering their function in the circuit to achieve better circuit specifications. Now, if we can convert the operating plane given in Fig.7 into a graphical analysis plane including charts that show the behavior of all the specifications of MOS devices from WI to SI, the designer will see operating plane with more numerical and visual details. As shown in the right side of the Fig. 6, for the selected drain current and channel length, all specifications of the MOS devices mentioned in section 2.1.4 are simultaneously swept versus the IC in the graphical analysis section of the developed tool. This means that in addition to the numerical observation of all the specifications of MOS devices for three degrees of freedom, these parameters also can be seen for all channel ICs from WI to SI. So, designer can select the optimum ICs for MOS devices. The ability of activating critical inversion coefficient is also considered in the charts by red color so that designer can clearly observes the allowed regions of inversion of MOS devices to avoid from small geometry effects. If the designer intends to observe several specifications versus IC on a unit chart in order to optimization of multiple specifications simultaneously, an independent chart for activating of several characteristics has been also considered at the end of the graphical analysis section (this chart can be seen in Fig.3).

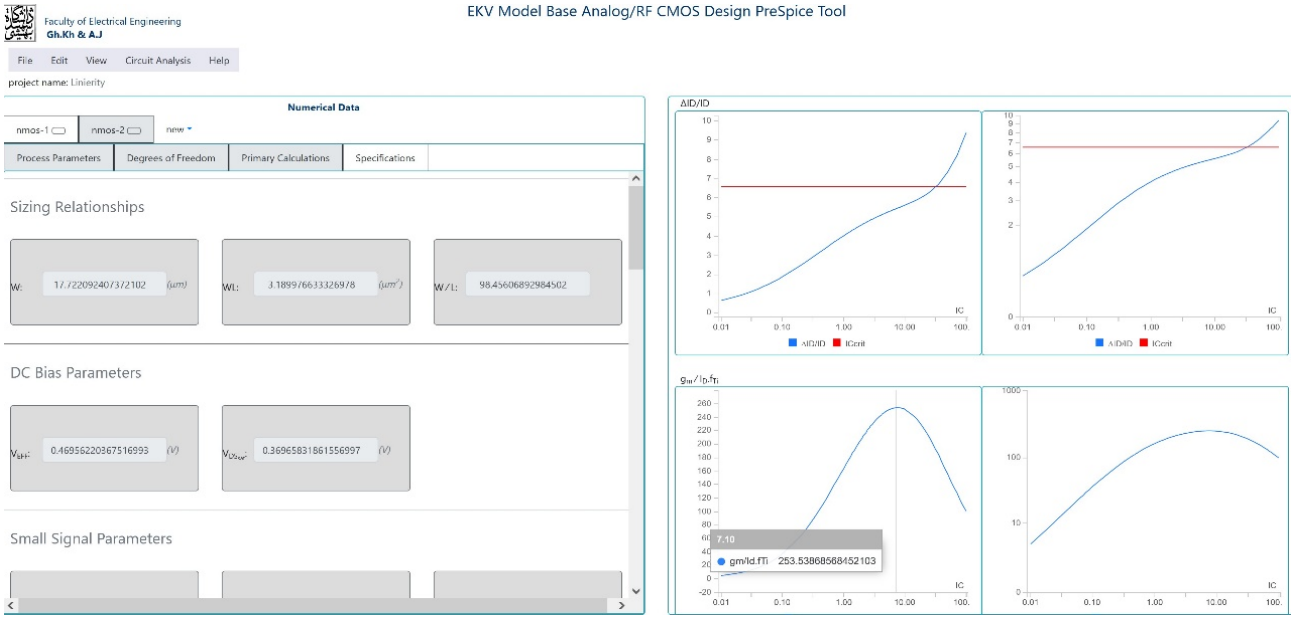

Fig 6. A small part of the tool's specifications section.

Table 3. Device specifications in analog/RF CMOS design Pre–SPICE tool.

Specification	Equation	Description	Unit
Sizing Relationships	$\mathrm{W} = \left(\frac{\mathrm{L}}{\mathrm{IC}}\right).\left(\frac{\mathrm{I_D}}{\mathrm{I_0}}\right)$	Width	µm
	$WL = (\frac{L^2}{IC})(\frac{I_D}{I_0})$	Gate Area	μm^2
	$\frac{W}{L} = (\frac{1}{IC})(\frac{I_D}{I_0})$	Shape Factor	--
DC Bias Parameters	$\mathrm{V_{EFF}} = 2\mathrm{nU_T}\ln\left(\mathrm{e}^{\sqrt{\mathrm{A}}} - 1\right)$	Effective Gate-Source Voltage	V
	$V_{DS_{sat}} = 2U_T\sqrt{IC + 0.25} + 3U_T$	Drain-Source Saturation Voltage	V
Small Signal Parameters	$\frac{\mathrm{g_m}}{\mathrm{I_D}} = \frac{1}{\mathrm{nU_T}\left(\sqrt{\mathrm{B} + 0.25} + 0.5\right)}$	Transconductance Efficiency	V^{-1}
	$\frac{g_{ds}}{I_D} = \frac{1}{V_A + V_{DS}}$	Drain-Source Conductance Efficiency	V^{-1}
	$\mathrm{g_m} = \left(\frac{\mathrm{g_m}}{\mathrm{I_D}}\right).\mathrm{I_D}$	Transconductance	µS
	$g_{ds} = \left(\frac{g_{ds}}{I_D}\right).\mathrm{I_D}$	Drain-Source Conductance	µS
	$g_{mb} = \eta.\mathrm{g_m}$	Body Effect Transconductance	µS
	$r_{ds} = (g_{ds})^{-1}$	Drain-Source resistance	KΩ
	$A_{1dB}(WI) = 1.22(nU_T)$	Input 1dB Compression Voltage for a Differential Pair in WI Region	V
	$A_{1dB}(SI) = 1.81(nU_T\sqrt{B})$	Input 1dB Compression Voltage for a Differential Pair in SI Region	V
Gain & Bandwidth Relationships	$V_A = \mathrm{V_A(CLM)} \parallel \mathrm{V_A(DIBL)}$	Early Voltage	V
	$A_{Vi} = \frac{V_A}{nU_T(\sqrt{B + 0.25} + 0.5)}$	Intrinsic Voltage Gain	--
	$f_{Ti} = (\frac{IC}{\sqrt{B + 0.25} + 0.5})(\frac{\mu U_T}{\pi(\widehat{\mathrm{C_{gsi}}} + \widehat{\mathrm{C_{gbi}}})L^2})$	Intrinsic Bandwidth	GHZ
	$f_T = \frac{g_m}{2\pi(\mathrm{C_{gsi}} + \mathrm{C_{gbi}})}$	Bandwidth	GHZ
Gate Referred Thermal & Flicker Noise	$S_{VG} = 4KT(n\Gamma\sqrt{B + 0.25} + 0.5)(\frac{nU_T}{I_D})$	Gate Referred Thermal Noise Voltage PSD1	nV^2/HZ
	$\sqrt{S_{VG}} = \sqrt{4KT(n\Gamma\sqrt{B + 0.25} + 0.5)(\frac{nU_T}{I_D})}$	Square Root of Gate Referred Thermal Noise Voltage PSD	$nV/\sqrt{HZ}$
	$S_{VG}(f) = (\frac{IC}{L^2})(\frac{I_0}{I_D})\frac{K_F}{{C_{OX}}^2 f^{AF}}$	Gate Referred Flicker Noise Voltage PSD	nV^2/HZ
	$\sqrt{S_{VG}(f)} = \sqrt{(\frac{IC}{L^2})(\frac{I_0}{I_D})\frac{K_F}{{C_{OX}}^2 f^{AF}}}$	Square Root of Gate Referred Flicker Noise Voltage PSD	$nV/\sqrt{HZ}$
	$f_C = [\frac{2\pi K_F}{4KTC_{OX}}(\frac{\widehat{\mathrm{C_{gsi}}} + \widehat{\mathrm{C_{gbi}}}}{n\Gamma})]^{\frac{1}{AF}}$	Corner Frequency	GHZ
Local Area DC Mismatch	$\Delta V_T = AV_{T0}(1 + \frac{V_{SB}}{2\varphi_0})(\frac{\sqrt{IC}}{L}.\sqrt{\frac{I_0}{I_D}})$	Threshold Voltage Mismatch	mV
	$\frac{\Delta K_P}{K_P} = A_{KP}(\frac{\sqrt{IC}}{L}.\sqrt{\frac{I_0}{I_D}})$	Relative Transconductance Mismatch	--
	$\Delta V_{GS} = \left(\frac{\sqrt{IC}}{L}.\sqrt{\frac{I_0}{I_D}}\right).\sqrt{AV_T{}^2 + [A_{KP}nU_T(\sqrt{B + 0.25} + 0.5)]^2}$	Gate-Source Voltage Mismatch	mV
	$\frac{\Delta I_D}{I_D} = \left(\frac{\sqrt{IC}}{L}.\sqrt{\frac{I_0}{I_D}}\right).\sqrt{(\frac{AV_T}{nU_T(\sqrt{B + 0.25} + 0.5)})^2 + {A_{KP}}^2}$	Relative Drain Current Mismatch	--
Gate-Source Leakage Current	$I_{(GS)_L} = (\left(\frac{L^2}{IC}\right)\left(\frac{I_D}{I_0}\right)K_{GA}\left[nU_T\ln\left(1 + e^{\frac{V_{EFF}}{nU_T}}\right)\right]V_{GS}e^{K_{GB}.V_{GS}})$	Gate-Source Leakage Current	µA
Figure of Merits	$\left(\frac{\mathrm{g_m}}{\mathrm{I_D}}.f_{Ti}\right) = (\frac{1}{\mathrm{nU_T}\left(\sqrt{\mathrm{B} + 0.25} + 0.5\right)})((\frac{IC}{\sqrt{B + 0.25} + 0.5})(\frac{\mu U_T}{\pi(\widehat{\mathrm{C_{gsi}}} + \widehat{\mathrm{C_{gbi}}})L^2}))$	Low Power RF Design Figure of Merit	$V^{-1}GHZ$
	$(A_{Vi}.f_{Ti}) = (\frac{V_A}{nU_T(\sqrt{B + 0.25} + 0.5)})((\frac{IC}{\sqrt{B + 0.25} + 0.5})(\frac{\mu U_T}{\pi(\widehat{\mathrm{C_{gsi}}} + \widehat{\mathrm{C_{gbi}}})L^2}))$	Intrinsic Gain Bandwidth	GHZ
	$K = 1.380649 * 10^{-23}$ is Boltzmann Constant.		

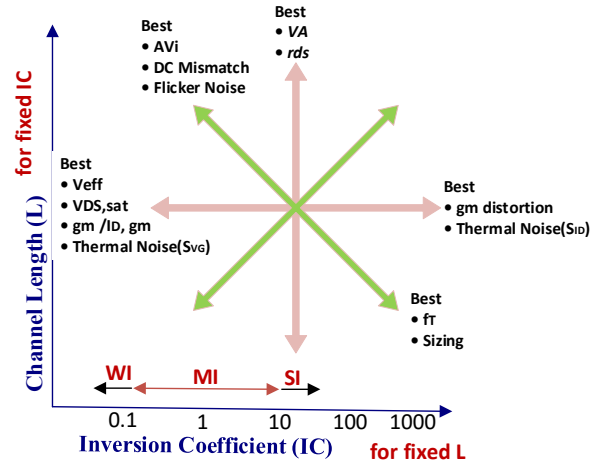

Fig 7. MOSFET operating plane versus selected inversion coefficient and channel length for a fixed drain current.

2.3 Circuit Analysis

Since this Pre-SPICE tool was developed to analyze and optimize the characteristics of analog/RF circuits, it also includes a section titled circuit analysis. As shown in Fig.8, all the relationships related to the characteristics of an analog/RF circuit including gain, bandwidth, noise figure, scattering parameters, phase noise, etc., can be rewritten using the process parameters (Table. 1), degrees of freedom (Table. 2), device specifications (Table. 3) and passive elements (resistor, capacitor, inductor). After saving these relationships as a circuit characteristic, the initial values are obtained automatically depending on the initial choices of degrees of freedom. By choosing and changing the degrees of freedom circuit devices, the designer, in addition to monitoring the characteristics of the devices in both numerical and graphical views, can also see the values and changes of the circuit characteristics in all inversion regions from weak to strong. Also, at each stage of the design, reporting from all of the information of the sections in CSV format is provided by this tool.

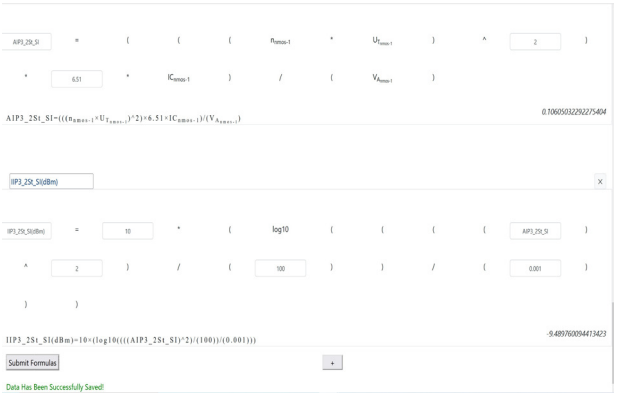

Fig 8. A small part of the tool's circuit analysis section.

3 Illustration of the EKV model base Analog/RF CMOS Design Pre-SPICE Tool Performance

To show the capability of this tool in pre-SPICE design, we will examine its performance in optimizing the linearity characteristic of one and two-stage differential amplifiers and a single ended OTA.

3.1 One Stage Differential Amplifier

Fig.9 illustrates a one-stage differential amplifier. According to the V_{EFF} relationship in the EKV model, $V_{EFF} = 2nU_T \ln\left(e^{\sqrt{IC}} - 1\right)$, the input voltage difference, ΔV_{in}, is as follow

$$\Delta V_{in} \approx 2nU_T[ln(e^{\sqrt{IC_1}} - 1) - ln(e^{\sqrt{IC_2}} - 1)] \quad (5)$$

where IC_1 and IC_2 are the ICs of the transistors M1 and M2, respectively. Assuming the bias of the transistors in the WI region ($IC < 0.1$) and using the Maclaurin expansion, (5) is given by

$$IC_1 - IC_2 \approx IC_2 \frac{\Delta V_{in}}{nU_T} + IC_2 \frac{(\Delta V_{in})^2}{2(nU_T)^2} + IC_2 \frac{(\Delta V_{in})^3}{6(nU_T)^3} + \cdots (6)$$

According to the relationship of the g_m/I_D in the WI region, $g_m/I_D = 1/nU_T$, and with the equal geometry of the transistors, output voltage difference, $\Delta V_{OUT} = \Delta I_D R_D$, is given by

$$\Delta V_{OUT} \approx g_{m2} R_D \Delta V_{in} + g_{m2} R_D \frac{(\Delta V_{in})^2}{2nU_T} + g_{m2} R_D \frac{(\Delta V_{in})^3}{6(nU_T)^2} + \ldots \quad (7)$$

So, the linearity indicator is given by

$$AIP3_{WI-1St} = \sqrt{\frac{4}{3}\left|\left(\frac{\alpha 1}{\alpha 3}\right)\right|} = 2.82\, nU_T \approx 3nU_T \quad (8)$$

It is observed that the AIP3 is almost constant in the WI region.

Assuming the bias of the transistors in the SI region (IC > 10), (5) is given by

$$IC_1 - IC_2 = \frac{\Delta V_{in}}{2nU_T} \sqrt{2(IC_1 + IC_2)\left(1 - \frac{(\frac{\Delta V_{in}}{2nU_T})^2}{2(IC_1 + IC_2)}\right)} \quad (9)$$

Since, $(\frac{\Delta V_{in}}{2nU_T})^2 \ll 2(IC_1 + IC_2)$, and with the equal geometry of the transistors, output voltage difference is given by

$$\Delta V_{OUT} \approx \frac{I_{spec} R_D}{2nU_T} \sqrt{2(IC_1 + IC_2)} \Delta V_{in} - \frac{I_{spec} R_D}{4(2nU_T)^3} \frac{\sqrt{2(IC_1 + IC_2)}}{(IC_1 + IC_2)} \Delta V_{in}^3 \quad (10)$$

So, linearity indicator, is given by

$$AIP3_{SI-1St} = \sqrt{\frac{4}{3}\left|\left(\frac{\alpha 1}{\alpha 3}\right)\right|} \approx 4.61nU_T\sqrt{(IC_1 + IC_2)} \quad (11)$$

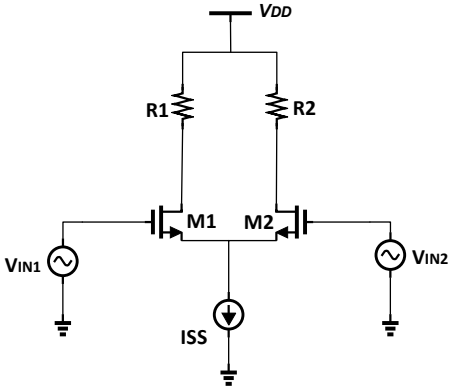

Fig 9. Single stage Differential Amplifier.

It is observed that the linearity of the circuit is proportional to inversion coefficients of the two transistors. Assuming, $IC_1 = IC_2 = IC$, relation (11) is given by

$$AIP3_{SI-1St} = \approx 6.51nU_T\sqrt{(IC)} \quad (12)$$

As a result, the linearity in the SI region is proportional to inversion coefficient. By increasing the inversion coefficient of the transistors, the linear performance of the circuit improves, but when the value of IC exceeds the value of IC_{CRIT}, we will face small geometry effects. When $IC < IC_{CRIT}$, small geometry effects are negligible, but when $IC > IC_{CRIT}$, these effects can't be ignored and transconductance efficiency decreases significantly in SI and consequently this lowers intrinsic voltage gain and bandwidth. In deep SI ($IC \gg 10$), V_{EFF} is defined by [13]

$$V_{EFF} = \frac{(2nU_T)^2}{\left(LE_{CRIT} \| \frac{1}{\theta}\right)} IC \quad (13)$$

Using (13), difference of ICs in (9) is given by

$$IC_1 - IC_2 = \frac{\Delta V_{in}\left(LE_{CRIT} \| \frac{1}{\theta}\right)}{(2nU_T)^2} \quad (14)$$

So, AIP3 will have infinite values and consequently the circuit behavior will be linear, but as explained, for ICs higher than IC_{CRIT}, we will face the problems of small geometry effects. Therefore, the optimal operating points of transistors for achieving high linearity is IC_{CRIT}. It should be noted that in processes smaller than 0.18μm, the value of IC_{CRIT} is smaller and according with relation (15), at L = 20nm its value will be about 1 [26]. So, the operating points will be done in the middle of the MI that usually for low power designs is an optimal point.

$$IC_{CRIT} \approx \left(\frac{L_{min}}{20nm}\right)^2 \quad (15)$$

3.2 Two Stage Differential Amplifier

Fig.10 shows the general block diagram of a two-stage differential amplifier by assuming nonlinear effects up to

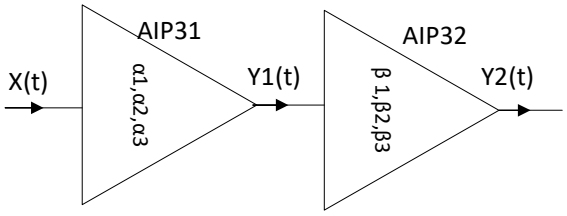

Fig 10. Two-stagE DifferentialAmplifier.

third order. Assuming full symmetry of the circuit and eliminating the second harmonic effect, linearity indicator is given by [27]:

$$\frac{1}{AIP3^2} \approx \frac{1}{AIP3_1^2} + \frac{\alpha_1^2}{AIP3_2^2} \quad (16)$$

where AIP3 is linearity indicator of total circuit and $AIP3_1$ and $AIP3_2$ are linearity indices of first and second stage of circuit respectively. Assuming the bias of the transistors in the WI region, the AIP3 is given by

$$AIP3_{WI-2St} \approx \sqrt{\frac{(2.828nU_T)^2}{1+\alpha_1^2}} \quad (17)$$

where $AIP3_{WI-2St}$ and α_1 are the AIP3 of two stage differential amplifier in WI region and the first stage intrinsic gain of circuit respectively. Intrinsic gain of differential amplifier is defined

$$\alpha_1 = g_m r_O = \frac{g_m}{I_D} . I_D . \frac{V_A}{I_D} = \frac{g_m}{I_D} . V_A \quad (18)$$

where V_A is Early voltage of transistors. By replacing $g_m/I_D = 1/nU_T$ in (18), AIP3 is given by

$$AIP3_{WI-2St} \approx \frac{2.828(nU_T)^2}{V_A} \quad (19)$$

In the EKV model, the value of VA is defined by [5]

$$V_A = V_A(CLM) \parallel V_A(DIBL) \quad (20\text{-a})$$

$$V_A(CLM) = V_{AL} . L \quad (20\text{-b})$$

$$V_A(DIBL) = \frac{1}{g_m/I_D\left[-DVT_{DIBL}.\left(L_{min}/L\right)^{DVT_{DIBLEXP}}\right]} \quad (20\text{-c})$$

where V_A(CLM) and V_A(DIBL) are Early voltages caused by CLM (channel length modulation) and DIBL (drain induced barrier lowering) effects respectively. Also DVT_{DIBL} and $DVT_{DIBLEXP}$ are process parameters. It is observed that, AIP3 is inversely proportional to VA. Fig. 11 illustrates the evolution of the Early voltage versus IC for an L = 0.18μm, nMOS device in a 0.18μm CMOS process. At IC=0.1, the Early voltage has a maximum value ($V_A = 1.68v$). Therefore, the minimum value of AIP3 is given by

$$AIP3_{WI-2St-min} \approx 1.683(nU_T)^2 \approx 2.04\,mV \qquad (21)$$

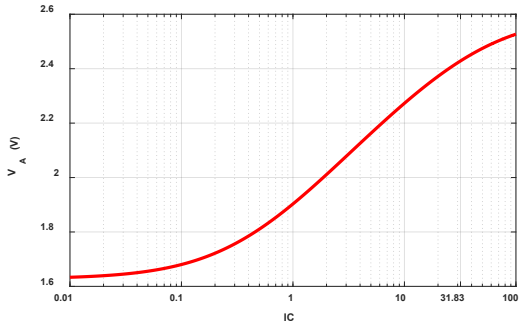

Fig 11. Evolution of Early voltage versus IC for an L = 0.18µm, nMOS device in a 0.18µm CMOS process.

That's mean in the WI region, the minimum value of the third order input intercept point, IIP3, approximately is -43dBm.

Fig.12, shows IIP3 versus IC for 1-stage and two-stage differential amplifiers in the WI region. IIP3 values are almost constant in both amplifiers. As expected, IIP3 value of the two-stage amplifier approximately 33dB lower than the single-stage amplifier.

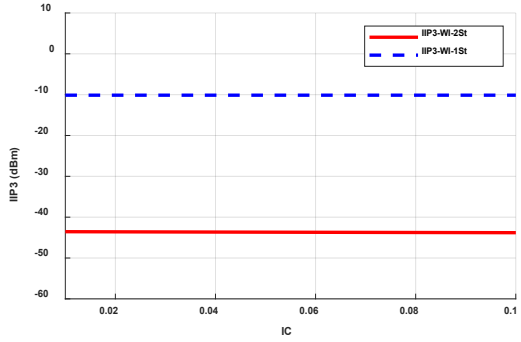

Fig 12. IIP3 measurement of 1stage and 2stage differential amplifiers in WI region in a 0.18µm process.

Assuming the bias of the transistors in the SI region and $IC_1 = IC_2 = IC$, the linearity indicator is given by

$$AIP3_{SI-2St} \approx \sqrt{\frac{\left(6.51nU_T\sqrt{IC}\right)^2}{1+\alpha_1^2}} \qquad (22)$$

where $AIP3_{SI-2St}$ is the linearity indicator of two stage differential amplifier in the SI. By replacing the α_1 of the first stage and the g_m/I_D in SI region, $g_m/I_D = 1/nU_T\sqrt{IC}$, $AIP3_{SI-2St}$ is given by

$$AIP3_{SI-2St} \approx \frac{6.51(nU_T)^2 IC}{V_A} \qquad (23)$$

Fig.13, shows the IIP3 versus IC for 1-stage and two-stage differential amplifiers in SI region. As expected, the IIP3 value of the two-stage circuit is approximately 21.5dB lower than the one-stage circuit. As mentioned in section 3.1, in deep SI, AIP3 will has infinite value and

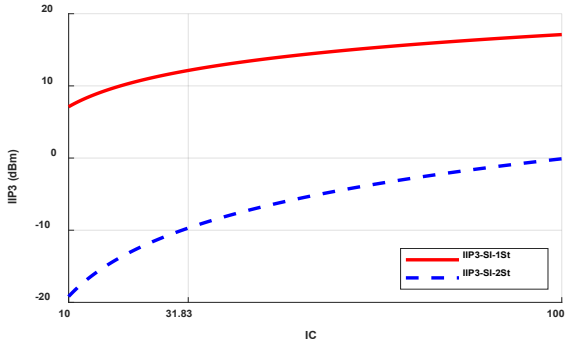

Fig 13. IIP3 measurement of 1-stage and 2-stage differential amplifiers SI region in a 0.18µm CMOS process.

the circuit behavior will be linear, but as explained again in section 3.1, for $IC > IC_{CRIT}$, we will face the problems of short channel effects. So again, the optimal operating points of transistors for achieving high linearity is IC_{CRIT}.

As shown in Fig.11, at $IC_{CRIT} = 31.83$, the value of Early voltage is $V_A = 2.4285V$. Therefore, the optimal value of AIP3 and IIP3 is given by

$$AIP3_{SI-2St-OPTIMUM} \approx 84.57(nU_T)^2 \approx 0.1V \qquad (24\text{-a})$$

$$IIP3_{SI-2St-OPTIMUM} \approx -10dBm \qquad (24\text{-b})$$

3.3 Design Methodology

The IC_{CRIT} calculation allows to find the optimal biasing and the linearity indicator (Section. 3). With this approach we can realize a complete design methodology represented in Fig. 14:

Step 1. Generation g_m/I_D vs IC to finding IC_{CRIT} (Fig. 5).

Step 2. Determine the channel length. To obtain better performance is set to the minimum $L_{min} = 0.18\mu m$.

Step 3. Generation V_A vs IC to finding V_A at IC_{CRIT} (Fig. 11).

Step 4. Generation drain-source conductance, g_{dso}, vs IC to finding g_{dso} at IC_{CRIT} (Fig. 15).

Step 5. Computation I_D using $I_D = V_A g_{dso}$.

Step 6. Computation gate-source voltage, V_{GS}, using

$$V_{GS} = 2nU_T \ln\left(e^{\sqrt{A}} - 1\right) + V_{TH} \qquad (25)$$

Step 7. Computation W/L using $W/L = I_D/IC_{CRIT} \cdot I_0$.

Step 8. Computation W using $W = (L/IC_{CRIT}) \cdot (I_D/I_0)$.

Step 9. Rewriting the IIP3 in the circuit analysis section of Analog/RF CMOS Design Pre-SPICE Tool.

As shown in design flow at Fig. 14, all of mentioned steps is done automatically in Analog/RF CMOS Design Pre-SPICE Tool.

3.4 Single-ended OTA

Fig. 16 illustrates a single-ended OTA circuit with a pMOS current mirror as the load and an nMOS current mirror as the current source. In this section, we will design the circuit based on the characteristics outlined in Table 4 using the Pre-SPICE tool.

Assuming $g_{m_3}(r_{ds_1} \parallel r_{ds_3}) \gg 1$, the differential voltage gain, A_{vd}, common-mode voltage gain, A_{vc}, and the gain-bandwidth product, GBW, are calculated as follows:

$$A_{vd} = V_{out}/V_{id} \cong g_{m_1}/(g_{ds_2} + g_{ds_4}) = \left(\frac{g_m}{I_D}\right)_1 \times (V_{A2} \parallel V_{A4}) \quad (26)$$

$$A_{vc} = V_{out}/V_{ic} \cong g_{ds_5}/2g_{m_3} \quad (27)$$

$$GBW \cong g_{m_1}/2\pi C_L \geq 100MHz \rightarrow g_{m_1} \geq 628\mu s \quad (28)$$

where g_{m_1}, g_{ds_2}, g_{ds_4}, $(g_m/I_D)_1$, V_{A2}, V_{A4}, g_{ds_5}, and g_{m_3} are the conductance of M1, the drain-source conductance of M2 and M4, the transconductance efficiency of M1, the Early voltage of M2 and M4, the drain-source conductance of M5, and the conductance of M3, respectively.

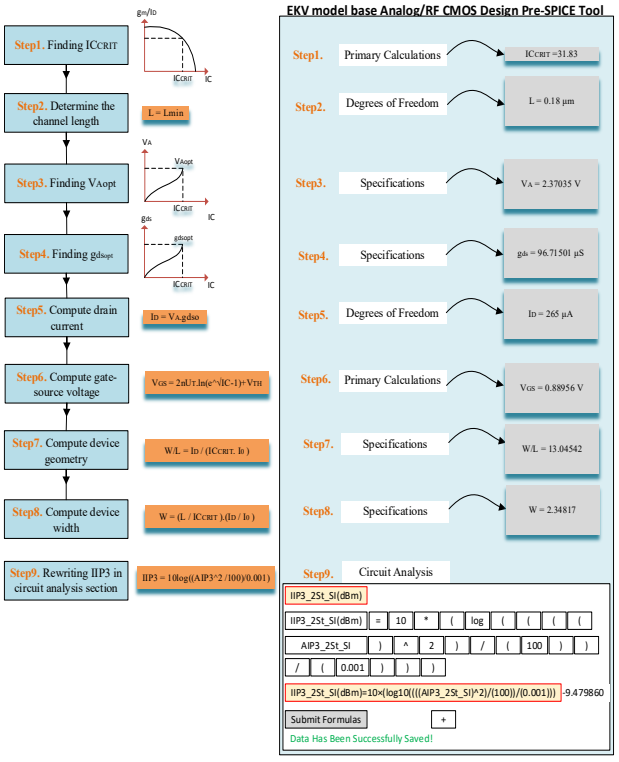

Fig 14. Complete design flow of linearity indicator optimization.

Table 4. OTA predefined characteristics.

Design Parameters	Description	Range
I_{BIAS}	Bias Current	$\leq 100\mu A$
A_{vd}	Differential Voltage Gain	$\geq 35dB$
C_L	Load Capacitance	1pF
GBW	Gain Bandwidth Product	$\geq 100MHz$
UGF	Unity Gain Frequency	$\geq 100MHz$

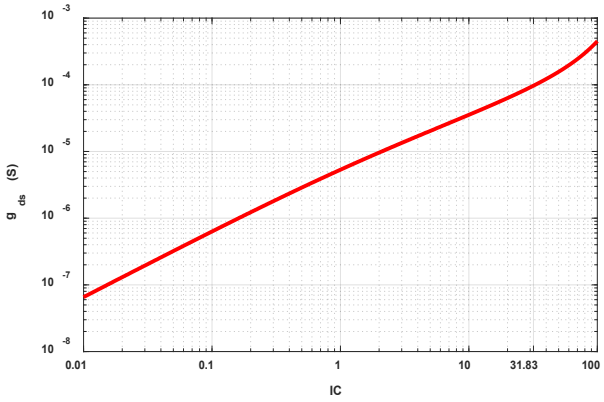

Fig 15. Evolution of drain-source conductance versus IC for an L = 0.18µm, nMOS device in a 0.18µm CMOS process.

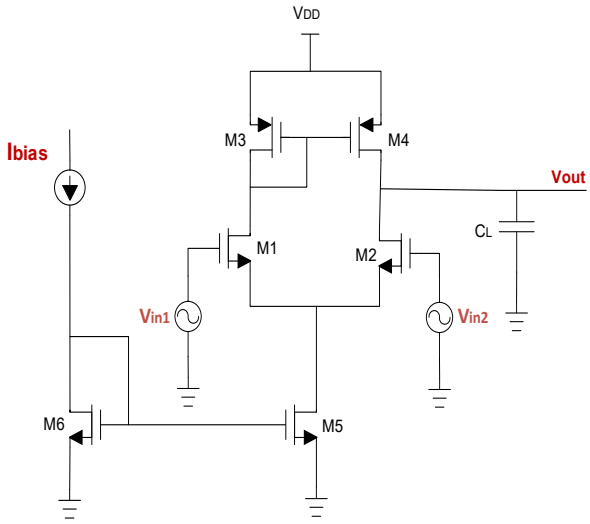

Fig 16. Single-ended operational transconductance amplifier (OTA).

The presence of g_{ds_4} in the denominator of the A_{vd} results in a 50% reduction in differential voltage gain (assuming equal drain-source conductivities of M2 and M4). Therefore, g_{ds_4} should be minimized or its associated Early voltage, $g_{ds_4} = I_{D4}/V_{A4}$, increased. This indicates that differential voltage gain largely depends on the intrinsic gain of M1 and the Early voltage of M4. To make tradeoff between differential voltage gain and bandwidth while selecting optimal values for L, IC, and I_D, Fig. 17 shows the intrinsic gain

and bandwidth of the input nMOS transistors versus IC for channel lengths ranging from 0.18µm to 1.08µm. By selecting the channel length as a multiple of the L_{min} and the inversion coefficient in the MI region, the desired gain and bandwidth characteristics are achieved. Therefore, we choose moderate inversion region center, IC=1, and three times the minimum process channel length, 0.54µm, for the input nMOS transistors.

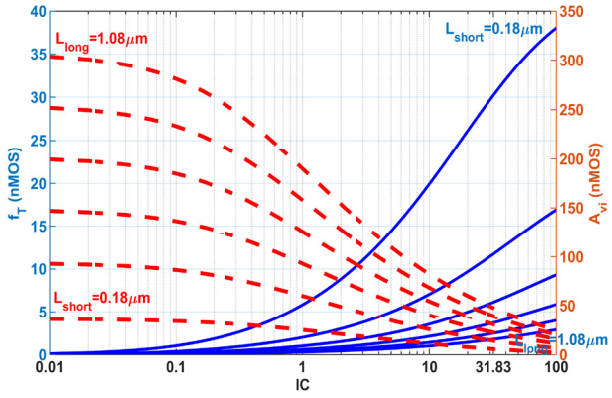

Fig 17. Bandwidth and intrinsic gain of input nMOS transistors versus IC for channel lengths from 0.18µm to 1.08µm.

By entering these values into the Pre-SPICE tool, the transconductance efficiency, $(g_m/I_D)_{1,2} = 17.708\,V^{-1}$, drain current, $I_{D1,2} = g_{m_{1,2}}/(g_m/I_D)_{1,2} \geq 34.5\mu A$, and channel width, $W_{1,2} = 31.303\mu m$, of M1 and M2 are automatically calculated and stored.

While g_{ds_2} and g_{ds_4} in the A_{vd} relation decrease the circuit's open-loop gain, they have minimal impact on GBW and UGF. It's essential that the sizes of the intrinsic and extrinsic capacitors of M3 and M4 do not influence GBW and UGF values. Therefore, biasing M3 and M4 in the SI region, where capacitor sizes are small, is more suitable. To minimize g_{ds_4}, the Early voltage of M4 should be maximized. As shown in Table 2, the Early voltage is a function of L; thus, selecting higher values for L and IC in M3 and M4 helps meet the circuit's required characteristics. Selecting a very large IC value increases V_{EFF}, which reduces headroom and output swing. Therefore, we choose IC = 12.5 and four times the minimum process channel length (0.72µm) for the pMOS load transistors. By entering these values into the Pre-SPICE tool, the transconductance efficiency, $(g_m/I_D)_{3,4} = 6.90\,V^{-1}$ and channel width, $W_{3,4} = 15.79\mu m$, of M3 and M4 are automatically calculated and stored.

To minimize the common-mode voltage gain, A_{vc}, the value of g_{ds_5} should be minimized or V_{A5} maximized. Therefore, selecting a large L for these transistors, M5, M6, is necessary (we also consider the channel length equal to that of transistors M3 and M4). According to Fig. 16, the drain-source voltage of M5 and M6 matches the source-body voltage of M3 and M4. To find the optimal IC value for a given L and V_{DS}, it suffices to calculate the maximum Early voltage of M5 and M6. Fig. 18 shows the evolution of the Early voltage of these transistors versus IC. It is clear from the figure that the maximum value of V_{A5} occurs at IC = 4.05. By entering these values into the Pre-SPICE tool, the transconductance efficiency, $(g_m/I_D)_{5,6} = 11.06\,V^{-1}$ and channel width, $W_{5,6} = 20.61\mu m$, of M5 and M6 are automatically calculated and stored.

After selecting the degrees of freedom for M1 to M6, all parameters and characteristics of these components are automatically calculated and saved in the Pre-SPICE tool. Additionally, the specifications of the circuit transistors are displayed in separate graphs versus IC for the selected channel length and drain current. This allows the designer to numerically observe all MOS device characteristics across three degrees of freedom and for all channel inversion coefficients, from weak to strong inversion, enabling the selection of operating points and device bias region based on predefined characteristics, applications, or standards.

Next, (26), (27), and (28) are rewritten in terms of the degrees of freedom of M1-M6 in the circuit analysis section of the Pre-SPICE tool:

$$A_{vd}(\overrightarrow{IC},\overrightarrow{L}) = \left(\frac{g_m}{I_D}\right)_1 . (V_{A2} \parallel V_{A4}) = f(IC_{1,3}, L_{1,3}) \quad (29)$$

$$A_{vc}(\overrightarrow{IC},\overrightarrow{L}) \cong \frac{\left(\frac{I_{D5}}{V_{A5}}\right)}{2\left(\frac{g_m}{I_D}\right)_4 . I_{D4}} = f(IC_{3,5}, L_{3,5}) \quad (30)$$

$$GBW(\overrightarrow{IC}) \cong \frac{\left(\frac{g_m}{I_D}\right)_1 . I_{D1}}{2\pi C_L} = f(IC_1) \quad (31)$$

The initial values of these characteristics are automatically calculated and stored in the circuit analysis section of the tool. Table 5 compares the initial values obtained from the Pre-SPICE tool with those from SPICE software (Cadence Virtuoso) against the predefined characteristics. As shown, the GBW value in the Pre-SPICE tool and the UGF value in the SPICE software do not match the predefined characteristics.

Rewriting (31) using the EKV model equations in Table 3 yields:

$$GBW(\overrightarrow{IC}) \cong \frac{I_{D1}}{nU_T 2\pi C_L\left(\sqrt{\left(IC_1\left(1+\frac{IC_1}{IC_{CRIT}}\right)\right)}+0.25+0.5\right)} \quad (32)$$

Reducing $IC_{1,2}$ clearly increases the GBW value. Thus, by adjusting the value of $IC_{1,2}$ from 1 to 0.75, the target characteristics are achieved. With this slight change accounted for in the degrees of freedom section of the Pre-SPICE tool, all processes related to primary

calculations, device specifications, and circuit analysis are automatically re-performed, and the results are saved.

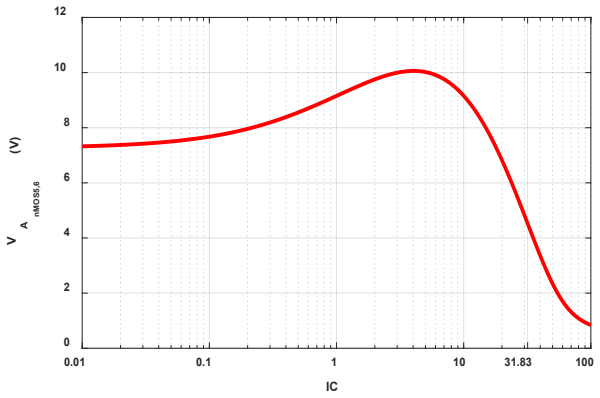

Fig 18. Evolution of the Early voltage of M5 and M6 versus IC for an L = 0.72µm, $V_{DS} = 0.413V$ nMOS device in a 0.18µm CMOS process.

Table 5. The initial values obtained from the Pre-SPICE tool with those from SPICE software (Cadence Virtuoso) against the predefined characteristics or goal spec.

Circuit Spec	Value in Pre-SPICE Tool	Satisfy	Value in SPICE Tool	Satisfy	Goal Spec
A_{vd} (dB)	40.143	Yes	41.062	Yes	≥ 35
I_{Bias} (μA)	37	Yes	36.53	Yes	≤ 100
GBW (MHz)	98.241	No	104.021	Yes	≥ 100
UGF (MHz)	---	---	97.96	No	≥ 100

Fig. 19 illustrates the variation of A_{vd} versus frequency in SPICE software (Cadence Virtuoso). Table 6 compares the values from the Pre-SPICE tool and SPICE software against the goal and predefined characteristics. All values obtained from both tools align with the predefined goal characteristics.

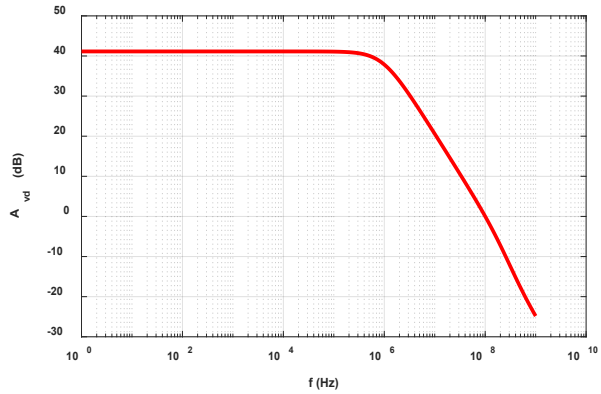

Fig 19. Differential voltage gain versus frequency in SPICE software (cadence Virtuoso) in a 0.18µm CMOS process.

Table 6. The final values obtained from the Pre-SPICE tool with those from SPICE software (Cadence Virtuoso) against the predefined characteristics or goal spec.

Circuit Spec	Value in Pre-SPICE Tool	Satisfy	Value in SPICE Tool	Satisfy	Goal Spec
A_{vd} (dB)	40.78	Yes	41.114	Yes	≥ 35
I_{Bias} (μA)	37	Yes	36.58	Yes	≤ 100
GBW (MHz)	105.06	Yes	107.6	Yes	≥ 100
UGF (MHz)	---	---	100.16	Yes	≥ 100

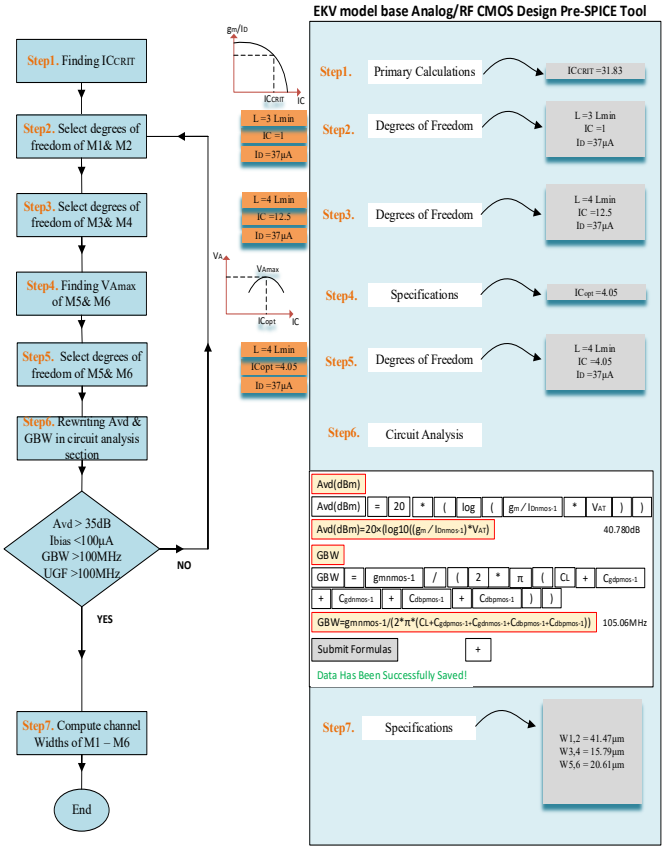

Fig 20. Complete design flow of an OTA design with predefined characteristics.

3.5 Design Methodology

Fig. 20 presents the complete OTA circuit design methodology, detailed as follows:

Step 1. Calculate of IC_{CRIT} for avoid of small geometry effects (Fig. 5).

Step 2. Select degrees of freedom of M1& M2 ($L = 3L_{min}, IC = 1, I_D = 37\mu A$).

Step 3. Select degrees of freedom of M3& M4 ($L = 4L_{min}, IC = 12.5, I_D = 37\mu A$).

Step 4. Generation V_A vs IC to finding V_{Amax} at IC_{opt} (Fig. 18).

Step 5. Select degrees of freedom of M5& M6 ($L = 4L_{min}$, $IC_{opt} = 4.05, I_D = 37\mu A$).

Step 6. Rewriting the A_{vd} and GBW in the circuit analysis section of Analog/RF CMOS design Pre-SPICE tool in terms of degrees of freedom of M1-M6.

Step 7. Calculate channel widths M1-M6 using $W = (L/IC_{CRIT}) . (I_D/I_0)$.

As shown in design flow at Fig. 20, all of mentioned steps is done automatically in Analog/RF CMOS Design Pre-SPICE Tool.

4 Simulation Validation

The results of the sizing algorithms presented in this paper are useful for pre-sizing the circuits. Then, the design variables have to be adjusted during CAD simulations. In this section, the proposed circuits (two-stage differential amplifier and OTA) are simulated in 0.18µm process from TSMC, in order to validate design methodologies.

As illustrated in Fig. 21, in the two-stage differential amplifier, the prediction of the IIP3 by the proposed methodology in all of the SI region is consistent with the simulation results. Fig. 22, shows the IIP3 measurement of the two-stage differential amplifier at $IC = IC_{CRIT}$. As shown, the value of -10.01dBm is completely consistent by the value of -10dBm extracted from prediction relationship (24).

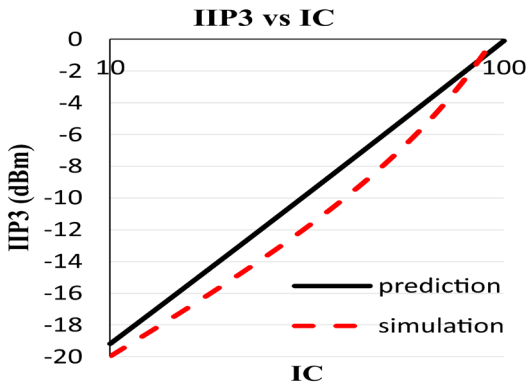

Fig 21. Prediction (full lines) and simulation (dotted lines) of IIP3 of the two-stage differential amplifier in SI region versus IC in 0.18µm CMOS process.

Fig. 23 shows that the prediction of the A_{vd} by the proposed methodology in all of the regions from WI to SI in the OTA circuit is consistent with the simulation results.

Figure 2 illustrates that the Pre-SPICE tool can generate CSV reports at any design stage. To be concise, Table 7 includes only a summary of the final report for the two-stage differential amplifier circuit in a 0.18µm CMOS process.

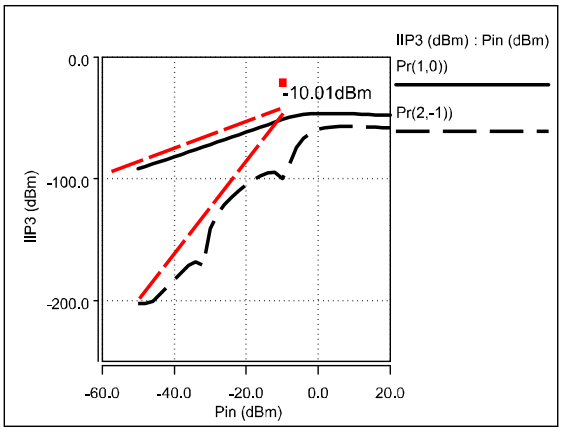

Fig 22. IIP3 versus input power in two-stage differential amplifier in 0.18µm CMOS process.

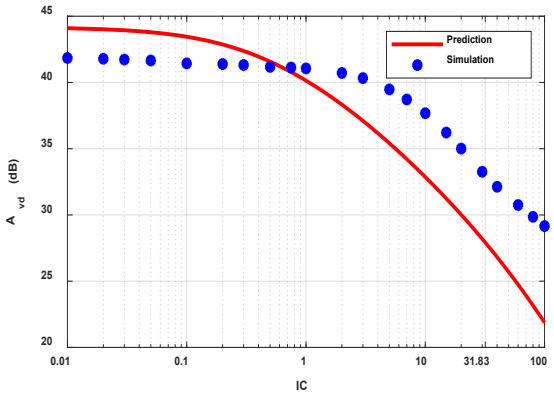

Fig 23. Prediction (full lines) and simulation (dotted lines) of A_{vd} of the OTA versus IC in 0.18µm CMOS process.

5 Conclusions

A new CAD tool for optimizing MOS drain current and sizing has been presented for use in any analog and RF circuit topology. This tool runs on all web browsers. The design methodologies reported in this paper offers many advantages for analog/RF circuit design. On one hand, these facilitate a simple and accurate design to optimize the circuit. On the other hand, by converting the operating plane shown in Fig. 7 into a graphical analysis page with charts displaying the behavior of all MOS device specifications from WI to SI, the designer can view this page in real time with enhanced numerical and visual details. These methodologies have proven effective in designing 1-stage and 2-stage differential amplifiers and an operational transconductance amplifier (OTA) circuit.

Table 7. summary of the final report for the two-stage differential amplifier circuit in a 0.18µm CMOS process.

EKV Model Base Analog/RF CMOS Design Pre-SPICE Tool Project Name: 2St Diff Amp								
Transistor 0: nmos-1 Type: nmos Technology: 180nm		Transistor 1: nmos-2 Type: nmos Technology: 180nm						
Process Parameters								
L_min	0.18	µm	LEXP	3	---	C_GS0V	0.94	fF/µm
t_ox	4.1	nm	DL	0.028	µm	C_GD0V	0.94	fF/µm
mu_n	422	$\mu A/V^2$	beta	0.8	---	C_GB0V	0	fF/µm
Y	0.56	$V^{1/2}$	K_F0	3.18E-31		C_gdi_hat	0	---
E_CRIT	5.6	V/µm	V_KF	1	V	f	1	HZ
alpha	1.3	---	AF	0.85	---	T	300	K
theta	0.28	V^{-1}	A_VT0	5	mV. µm	V_DD	1.8	V
n	1.35	---	A_KP	µm	µm	V_SB	0	V
V_T0	0.42	V	V_AL	14.44	V/µm	V_DS	0.25	V
BL	-8	mV/V	PHI_F	0.425	V	f_0	2.4	GHz
DW	0	µm	V_sat	90659.09	m/s			
Degrees of Freedom								
		L	0.18	µm	W	17.7220924	µm	
		IC	31.83	---	V_EFF	0.4695622	V	
		I_D	265	µA	GMdivID	3.38020508	V^{-1}	
Primary Calculations								
V_T	0.42	V	C_GOX	26.8424	fF	K_F	6.87E-31	C^2/cm^2
c_ox	8.4146341	$fF/\mu m^2$	X	0.1885	---	L_eff	0.124	µm
U_T	0.0258	V	C_gsi_hat	0.6038	---	W_eff	17.722092	µm
k	355.097	$\mu A/V^2$	C_gbi_hat	0.10271	---	PHI_0	0.9532	V
I_0	0.638191	µA	C_gsi	16.2079	fF	AV_T	5	mV. µm
LE_CRIT_P_min	0.786124	V	C_gbi	2.75711	fF	eta	0.35	---
LE_CRIT_P	0.786124	V	C_gso	16.6587	fF	V_GS	0.8895	V
V_A_CLM	2.6	V	C_gdo	16.6587	fF	K_GA	5.61E-25	$A/\mu m^2V^2$
IC_CRIT_min	31.83871	---	C_gbo	0	fF	K_GB	4.633	V^{-1}
IC_CRIT	31.83871	---	C_gs	32.8666	fF	L_sat	0.02401	µm
B	63.65129	---	C_gd	16.6587	fF	Lambda_c	0.13343	---
A	45.45393	---	C_gb	2.75711	fF	C_gdi	0	fF
V_A_DIBL	26.83617	V	gamma	0.66159	---			
Specifications								
W	17.72209	µm	r_ds	1.37000	KΩ	S_VGF	30390514	nV^2/HZ
WL	3.189976	μm^2	A_1dBWI	0.0424	V	S_VGF_sqrt	5512.7592	$nV/\sqrt{HZ}$
WdivL	98.45606	---	A_1dBSI	0.50296	V	f_c	0.00652	GHz
V_EFF	0.469562	V	V_A	2.37035	V	DV_T	2.79947	mV
V_DS_SAT	0.369658	V	AV_i	8.01227	---	DKpdivKp	1.11978	--
GMdivID	3.380205	V^{-1}	fT_i	56.7335	GHz	DV_GS	4.40244	mV
GDSdivID	0.364962	V^{-1}	f_T	30.2032	GHz	DIDdivID	1.46607	--
g_m	6760.410	µS	f_Tr	32.7368	GHz	I_GSL	4.61E-17	µA
g_ds	729.9246	µS	S_VG	2.19205	nV^2/HZ	GMIDFT	191.77104	V^{-1}GHZ
g_mb	2366.143	µS	S_VG_sqrt	1.48055	$nV/\sqrt{HZ}$	AVIFTI	454.56458	GHz
Circuit Analysis Section Details								
Spec 1: AIP3_1St_WI		**Spec 2: IIP3_1St_WI (dBm)**		**Spec 7: AIP3_2St_SI**				
AIP3_1St_WI	0.09822	IIP3_1St_WI (dBm)	-10.15594	AIP3_2St_SI	0.1060503			
Spec 3: AIP3_2St-WI		Spec 4: IIP3_2St_WI (dBm)		Spec 8: IIP3_2St_SI (dBm)				
AIP3_2St-WI	0.001443256	IIP3_2St_WI (dBm)	-46.81310	IIP3_2St_SI (dBm)	-9.48970			
Spec 5: AIP3_1St_SI		**Spec 6: IIP3_1St_SI (dBm)**						
AIP3_1St_SI	1.279242214	IIP3_1St_SI (dBm)	12.13905					

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