Dual Z-Source Network Dual-Input Dual-Output Inverter

S. M. Dehghan*, M. Mohamadian*, A. Yazdain*, A. H. Rajaei* and H. Zahedi**

Abstract: This paper presents a modified nine switch inverter with two inputs and two Z-source networks. This inverter has two DC inputs and two AC outputs. Input DC voltages can be boosted to the required level. Amplitude, frequency and phase of AC output voltages can be controlled, independently. The proposed converter can be used in applications with two unregulated DC sources, which require feeding two independent loads. Compared to the conventional structure, the proposed converter requires reduced number of semiconductor switches hence improved converter reliability and less volume. While the authors have already presented a similar inverter (single z-source network dual-input dual-output inverter) with the above features, new inverter has some differences in the topology, control strategy and operation. In this paper, a new control strategy of space vector modulation for the new inverter is proposed. Also a new switching method utilizing carrier-based modulation concept is presented for both dual (proposed) and single z-source network dual-input dual-output inverters. Performance of the proposed inverter is verified by simulation and experimental results.

Keywords: Power Converters, Space Vector Pulse Width Modulation (SVPWM), Z-Source Network, Hybrid Energy Systems, Multi Terminal Converters.

1 Introduction

There are applications where energy conversion is required from two independent variable DC sources into two independent variable frequency AC loads. An example of these applications is traction drive system with six-phase motor and two DC energy sources such as battery and fuel cell system [1]. Another example is hybrid energy sources such as solar energy and wind energy, connected to a grid and also feeding a local load [2]. Such energy conversion systems conventionally require two DC/DC and two DC/AC converters (Fig. 1). This configuration requires at least one switch for each DC/DC converter and 6 switches for each DC/AC converter which add up to total 14 switches.

In this paper a novel converter is proposed that performs the same power conversion goal with only 9 semiconductor switches. Compared to the conventional method, this configuration reduces the volume and requires only one controller (Digital Signal Processor) for the system. The drawback is more complex switching algorithm and increased rating of the semiconductor switches.

As the title of the paper suggests, this converter is a modified nine-switch inverter with two z-source networks in front. The z-source network including two inductors, two capacitors and one diode was first used as front-end boost converter of a conventional inverter in [3] (Fig. 2). This inverter called z-source inverter is used as an efficient power conditioner in DG systems [4] and electric vehicle [5].

Nine-switch inverter is a converter with two AC outputs but with only one DC input [6]. The nine-switch inverter is used as an AC/AC converter in [7, 8]. In [9], a z-source nine-switch inverter is proposed (Fig. 3).

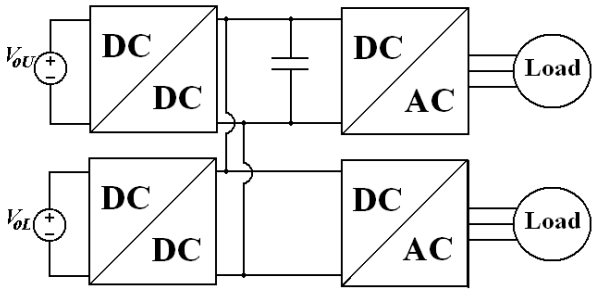


Fig. 1 Conventional power conversion architecture with two DC input and two AC outputs.

Iranian Journal of Electrical & Electronic Engineering, 2010.
Paper first received 26 Dec. 2009 and in revised form 2 Oct. 2010.
*The Authors are with the Department of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran.
E-mails: dehghansm@modares.ac.ir, mohamadian@modares.ac.ir, yazdian@modares.ac.ir, amir.h.rajaei@gmail.com
**The Author is with the Department of Electrical Engineering, Badrood Branch, Islamic Azad University, Badrood, Iran.
E-mail: zahedi13@yahoo.com.

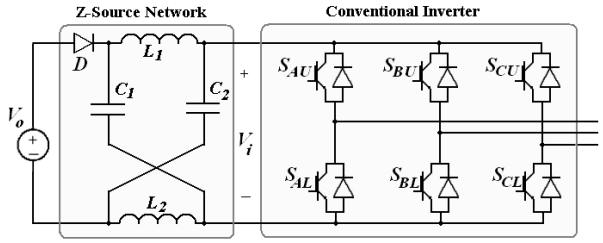


Fig. 2 Z-source inverter [3].

A single z-source network dual-input dual-output inverter (SZSN- DIDOI) has been proposed by the authors in [10] (Fig. 4). This inverter is composed of a modified nine switch inverter and a dual-input dual-output z-source network. As shown in Fig. 4, nine-switch inverter is modified with six extra diodes. Dual-input dual-output z-source network was first used in z-source three-level NPC inverter in [11].

In a single-input single-output z-source network, capacitors' voltages can be controlled and consequently input DC source is controllable. Since in Fig. 4, capacitors' voltages are related to both input DC sources; it is difficult to control the input voltages independently. However current control of input DC sources is possible [10]. As a solution a new nine-switch inverter is proposed in this paper (Fig. 5). In fact, dual-input dual-output z-source network is replaced by two single-input single output z-source networks. Using new topology, input voltages can be controlled independently.

This paper is organized as follows. Section 2 describes the modified nine-switch inverter. Section 3 describes operation of z-source networks in the proposed inverter. In sections 4, 5 and 6, space vector modulation, control strategy and PWM modulation are proposed for the new converter. Section 7 presents a comparison between the proposed inverter and SZSN-DIDOI. Finally, Section 8 describes simulation and experimental results.

2 Modified Nine-Switch Inverter

The modified nine-switch inverter is shown in Fig. 5. Extra Six diodes (D_{AU}, D_{BU}, D_{CU}, D_{AL}, D_{BL} and D_{CL}) are the difference between the nine-switch inverter and the modified nine-switch inverter. The modified nine-switch inverter is composed of two upper and lower inverters. Three upper switches, three mid switches and three lower extra diodes (D_{AL}, D_{BL} & D_{CL}) form the upper inverter. The output of the upper inverter is connected to the positive terminal of V_{iU} via upper switches and is connected to the negative terminal of V_{iU} via mid switches and lower extra diodes. The lower inverter includes three mid switches, three lower switches and three upper extra diodes (D_{AU}, D_{BU} & D_{CU}). The output of the inverter is connected to the positive terminal of V_{iL} via mid switches and upper extra diodes and connected to the negative terminal of

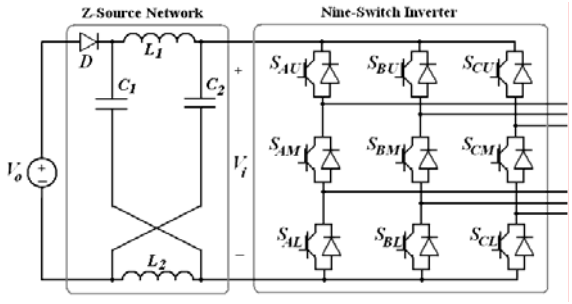


Fig. 3 Z-source nine-switch inverter [9].

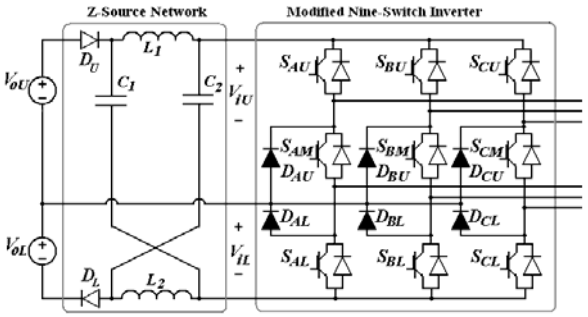


Fig. 4 Single z-source network dual-input dual-output inverter (SZSN-DIDOI) [10].

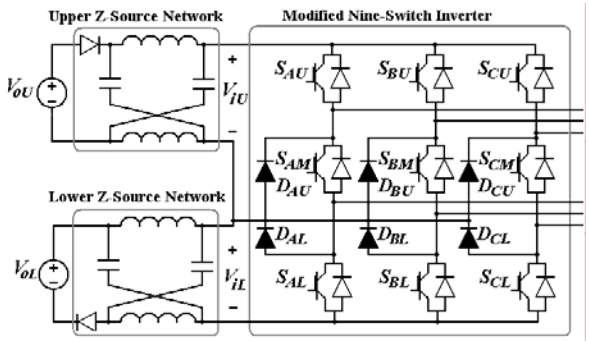


Fig. 5 Proposed dual z-source network dual-input dual-output inverter (DZSN-DIDOI).

V_{iL} via lower switches. In a conventional nine-switch inverter one of the outputs is in a zero switching vector state when the other output is in an active vector. However for the modified nine-switch inverter, in a similar situation, the DC input of the inverter in the zero vector state will be shorted. Therefore the modified nine-switch inverter requires necessarily a z-source network as front-end stage.

3 Operation of Z-Source Networks

In the proposed dual z-source network dual-input dual-output inverter (DZSN-DIDOI), two z-source networks are connected to the modified nine-switch inverter. The z-source networks can boost input DC voltages, as:

$$V_{iU} = B_U V_{oU} \quad (1)$$

$$V_{iL} = B_L V_{oL} \quad (2)$$

where V_{oU} and V_{oL} are input DC voltages and V_{iU} and V_{iL} are outputs of z-source networks. B_U and B_L are known as boost factors and are given by following equation [12]:

$$B_U = \frac{1}{1-2(T_{SCU}/T)} \quad (3)$$

$$B_L = \frac{1}{1-2(T_{SCL}/T)} \quad (4)$$

where T_{SCU} and T_{SCL} are the time intervals of shorting upper and lower z-source networks, respectively. The upper z-source network can be shorted across upper and mid switches and lower diode in a leg. However the lower z-source network can be shorted across lower and mid switches and upper diode in a leg.

4 Switching Method

A space vector modulation (SVM) method has been proposed for SZSN-DIDOI in [10] (Fig. 6). This SVM method can also used for the proposed DZSN-DIDOI. There are three types of switching vectors in one switching period: The active vectors for the upper inverter (V_1-V_6), the active vectors for the lower inverter (V_7-V_{12}), and the zero vectors (V_{13}-V_{16}). Regarding the reference signals the upper and lower active vectors are determined via diagrams of (b) and (c) in Fig. 6, respectively. All switching vectors for the proposed inverter are listed in Table 1. A leg may be in position {1}, {0}, {-1} or {2}. The states of the switches in these positions are illustrated by Table 2. Where, J could be A, B or C. The sign X indicates ON state of the diode over the active vectors and OFF state otherwise. The interval of switching vectors can be calculated as:

$$T_1 = \sqrt{3}\frac{V_{refU}}{V_{iU}} T \sin(\frac{\pi}{3} - \alpha_U) \quad (5)$$

$$T_2 = \sqrt{3}\frac{V_{refU}}{V_{iU}} T \sin(\alpha_U) \quad (6)$$

$$T_3 = \sqrt{3}\frac{V_{refL}}{V_{iL}} T \sin(\frac{\pi}{3} - \alpha_L) \quad (7)$$

$$T_4 = \sqrt{3}\frac{V_{refL}}{V_{iL}} T \sin(\alpha_L) \quad (8)$$

$$T_o = T - T_1 - T_2 - T_3 - T_4 \quad (9)$$

From Table 1, it is obvious that V_{iL} and V_{iU} are shorted over the upper and lower active vectors, respectively. For example during upper active vector of V_2, input V_{iL} is shorted across diode D_{CU} and switches S_{CM} and S_{CL}. This is not a problem, since over the upper active vectors; the lower inverter is in zero state and is not connected to its DC input and vice versa.

During time intervals of zero vectors both the upper and lower inverter are in the zero state. The zero vectors are divided to four groups depending on shoot-through state. V_{13} does not create any shoot-through state. V_{14} and V_{15} create shoot-through states for upper inverter

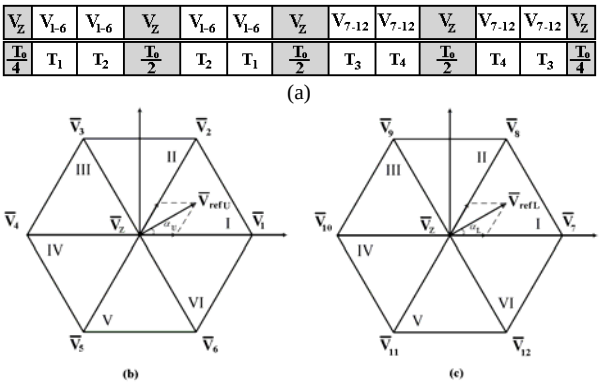


Fig. 6 SVM method for the presented inverter.

Table 1 Switching vectors of the presented inverter.

Vector	Leg A	Leg B	Leg C	Outputs		Shorted Input	
				Upper	Lower	Upper	Lower
1	1	0	0	Active	Zero	-	Yes
2	1	1	0				
3	0	1	0				
4	0	1	1				
5	0	0	1				
6	1	0	1				
7	-1	1	1	Zero	Active	Yes	-
8	-1	-1	1				
9	1	-1	1				
10	1	-1	-1				
11	1	1	-1				
12	-1	1	-1				
13	1	1	1	Zero	Zero	-	-
14	0	0	0	Zero	Zero	-	Yes
15	-1	-1	-1	Zero	Zero	Yes	-
16	2	2	2	Zero	Zero	Yes	Yes

Table 2 State of semiconductor devices in vectors defined by Table 1.

	S_{JU}	S_{JM}	S_{JL}	D_{JU}	D_{JL}
1	ON	OFF	ON	OFF	OFF
0	OFF	ON	ON	ON	X
-1	ON	ON	OFF	X	ON
2	ON	ON	ON	ON	ON

and lower inverter respectively. Vector V_{16} creates shoot-through states for both inverters. To create V_{16}, one of the legs must be in position {2} and other legs can be in position {1}, {0}, {-1} or {2}. The type of zero vectors can be selected based on control strategies and optimizations such as minimum number of semiconductor switching.

5 Control Strategy

The proposed inverter has several control variables (two modulation indices, two boost factors, four different zero vectors); therefore given output voltages can be implemented using some different approaches. Considering similar condition to SZSN-DIDOI, a simple control strategy based on capacitor voltage is presented in [10]. However, in this paper, a new control strategy based on voltage gains is proposed for the proposed DZSN-DIDOI. The output voltage gains G_U and G_L can be defined as [13, 14]:

$$G_U = 2\frac{V_{refU}}{V_{oU}} = m_U B_U \tag{10}$$

$$G_L = 2\frac{V_{refL}}{V_{oL}} = m_L B_L \tag{11}$$

Figure 7 shows the switching vectors used in this strategy. T_{ZN}, T_{ZL} and T_{ZU} are time intervals of V_{13}, V_{14} and V_{15}, respectively. In the proposed control strategy, the zero vectors V_{13}, V_{14} and V_{15} are used and vector V_{16} is disregarded. Therefore T_{SCU} and T_{SCL} are expressed by:

$$T_{SCU} = T_3 + T_4 + T_{ZU} \tag{12}$$

$$T_{SCL} = T_1 + T_2 + T_{ZL} \tag{13}$$

The aim of the control strategy is to determine time intervals of vectors in Fig. 7 based on given voltage gains. In the proposed control strategy, T_{SCU} and T_{SCL} are defined based on the modulation indices as:

$$T_{SCU} = \frac{\sqrt{3}}{2} m_L T + T_{EXU} \tag{14}$$

$$T_{SCL} = \frac{\sqrt{3}}{2} m_U T + T_{EXL} \tag{15}$$

where T_{EXU} and T_{EXL} are called extra shoot-through times. Thus using equations (3), (4), (10) and (11), the gains can be expressed by:

$$G_U = \frac{m_U}{1-\sqrt{3}\,m_L - 2(T_{EXU}/T)} \tag{16}$$

$$G_L = \frac{m_L}{1-\sqrt{3}\,m_U - 2(T_{EXL}/T)} \tag{17}$$

Solving (16) and (17) for m_U and m_L, yields:

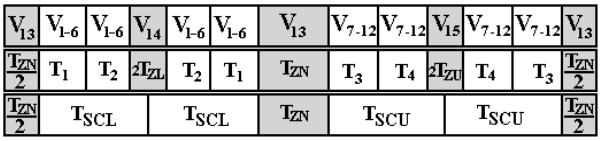


Fig. 7 Vectors and time intervals for proposed method based on voltage gains.

$$m_U = \frac{G_U\left(1-\sqrt{3}\,G_L - 2T_{EXU}/T + 2\sqrt{3}\,G_L T_{EXL}/T\right)}{1-3G_U G_L} \tag{18}$$

$$m_L = \frac{G_L\left(1-\sqrt{3}\,G_U - 2T_{EXL}/T + 2\sqrt{3}\,G_U T_{EXU}/T\right)}{1-3G_U G_L} \tag{19}$$

If T_{EXU} and T_{EXL} are given, the modulation indices would be determined. The denominator of equations (18) and (19) should be positive; satisfying the following constrains leads to:

$$0 < m_U < \frac{1+2T_{EXU}/T}{\sqrt{3}} \tag{20}$$

$$0 < m_L < \frac{1+2T_{EXL}/T}{\sqrt{3}} \tag{21}$$

According to Fig. 7, sum of T_{SCU} and T_{SCL} should be less than the switching cycle *T*. Therefore considering (14) and (15):

$$\left(\frac{\sqrt{3}\left(m_U + m_L\right)}{2} T + T_{EXU} + T_{EXL}\right) \le T \tag{22}$$

While T_{EXL} and T_{EXU} are zero, it can be shown if both voltage gains (G_U and G_L) are more than 0.577 or less than 0.577, equations (20-22) are satisfied. However if one of the gains is more and the other is less than 0.577, equations (20-22) are not satisfied. If G_U is larger than G_L, T_{EXL} can be set to zero and T_{EXU} is derived by the following value:

$$T_{EXU} = \left(0.5 - \frac{\sqrt{3}\,G_L}{4} - \frac{1}{4\sqrt{3}\,G_U}\right) T \tag{23}$$

Consequently*:*

$$m_U = 1/2\sqrt{3} \tag{24}$$

$$m_L = G_L/2 \tag{25}$$

Finally If G_L is the larger one, we can set T_{EXU} to zero and select T_{EXL} as:

$$T_{EXL} = \left(0.5 - \frac{\sqrt{3}\,G_U}{4} - \frac{1}{4\sqrt{3}\,G_L}\right) T \tag{26}$$

Thus*:*

$$m_U = G_U/2 \tag{27}$$

$$m_L = 1/2\sqrt{3} \quad (28)$$

Table 3 shows how to determine the modulation parameters using the voltages gains briefly. The modulation indices (m_U and m_L) and the extra shoot-through times (T_{EXU} and T_{EXL}) are determined via Table 3 for desired gains (G_U and G_L). Then time intervals of active vectors (T_1, T_2, T_3 and T_4) are calculated using equations (5-8). Finally the time intervals T_{ZU}, T_{ZL} and T_{ZN} are determined by following equations:

$$T_{ZU} = (\sqrt{3}/2)\, m_L\, T + T_{EXU} - T_3 - T_4 \quad (29)$$

$$T_{ZL} = (\sqrt{3}/2) m_U\, T + T_{EXL} - T_1 - T_2 \quad (30)$$

$$T_{ZN} = T - T_1 - T_2 - T_3 - T_4 - T_{ZU} - T_{ZL} \quad (31)$$

Also T_{SCU} and T_{SCL} can be calculated from (12) and (13) and consequently B_U and B_L, from (3) and (4). Fig. 8 shows the curves of the modulation indices for various gains.

6 Carrier-Based PWM

The proposed control strategy in the previous section can also be implemented by a carrier-based modulation. For this purpose, the following offset signals should be added to the upper and lower references signals:

$$\text{Offset}_U = 1 - \min(V_{aU}, V_{bU}, V_{cU}) - \sqrt{3} m_U - 2\frac{T_{EXL}}{T} \quad (32)$$

$$\text{Offset}_L = -1 - \max(V_{aL}, V_{bL}, V_{cL}) + \sqrt{3} m_L - 2\frac{T_{EXU}}{T} \quad (33)$$

Parameters m_U, m_L, T_{EXU} and T_{EXL} can be determined using Table 3. Fig. 9 shows the proposed PWM method. Similar to the conventional nine-switch inverter [6], by comparing the carrier signal with upper and lower reference signals, the gate signals are generated for the upper and lower switches, respectively.

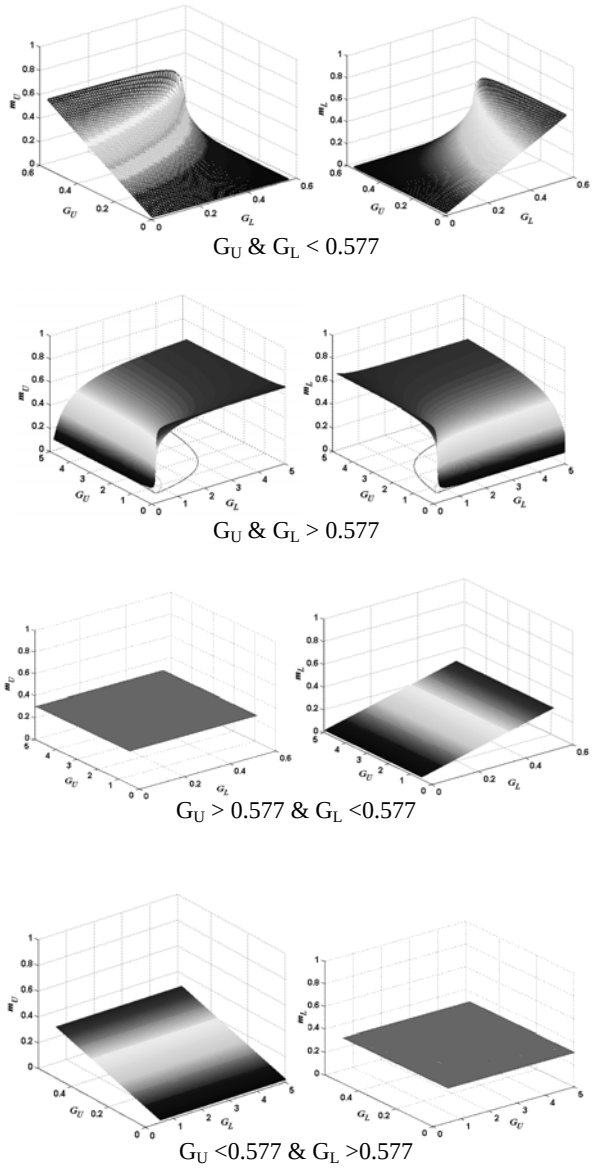


Fig. 8 The modulation indices in the proposed control strategy based on voltage gains.

Table 3 Determining modulation parameters based on voltage gains.

G_U	G_L	m_U	m_L	T_{EXU}	T_{EXL}
$< \frac{1}{\sqrt{3}}$	$< \frac{1}{\sqrt{3}}$	$\frac{G_U\left(1-\sqrt{3}G_L\right)}{1-3G_U G_L}$	$\frac{G_L\left(1-\sqrt{3}G_U\right)}{1-3G_U G_L}$	0	0
$> \frac{1}{\sqrt{3}}$	$< \frac{1}{\sqrt{3}}$	$\frac{1}{2\sqrt{3}}$	$\frac{G_L}{2}$	$\left(0.5 - \frac{\sqrt{3}G_L}{4} - \frac{1}{4\sqrt{3}G_U}\right)T$	0
$< \frac{1}{\sqrt{3}}$	$> \frac{1}{\sqrt{3}}$	$\frac{G_L}{2}$	$\frac{1}{2\sqrt{3}}$	0	$\left(0.5 - \frac{\sqrt{3}G_U}{4} - \frac{1}{4\sqrt{3}G_L}\right)T$
$> \frac{1}{\sqrt{3}}$	$> \frac{1}{\sqrt{3}}$	$\frac{G_U\left(1-\sqrt{3}G_L\right)}{1-3G_U G_L}$	$\frac{G_L\left(1-\sqrt{3}G_U\right)}{1-3G_U G_L}$	0	0

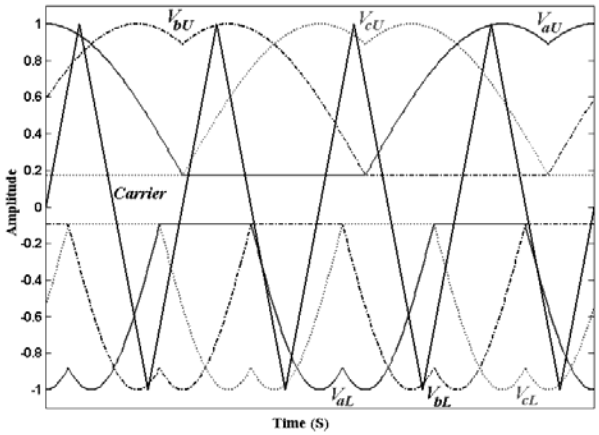


Fig. 9 Carrier-based PWM modulation for SZSN-DIDOI and DZSN-DIDOI.

The gate signals of the mid switches are generated by the logical XOR of the gate signals of upper and lower switches. As shown in Fig. 9, using the proposed offsets, minimum value of upper reference signals and maximum value of lower reference signals are always kept constant. In this manner T_{SCU} and T_{SCL} (and consequently B_U and B_L) are constant during fundamental cycle.

The carrier-based PWM can also be implemented for SZSN-DIDOI based on capacitor voltage control strategy presented in [10]. For this purpose, the above offset signals can be used for SZSN-DIDOI. However T_{EXU} and T_{EXL} are zero in this case.

7 Comparison

Both the proposed inverter (DZSN-DIDOI) and the inverter of Fig. 4 (SZSN-DIDOI) are dual-input dual-output inverters and can boost input voltages. However there are some differences between them.

DZSN-DIDOI acts as two independent z-source inverters. In this converter, upper z-source inverter is composed of three parts: upper DC input, upper z-source network and upper output, and similarly about lower z-source inverter. In other word, the power can be transferred from upper input to upper output and from lower input to lower output. Therefore if one of DC inputs disconnects, voltage of relevant output will be zero, however other output can continue normal operation.

Contrary to DZSN-DIDOI, SZSN-DIDOI (Fig. 4) cannot be considered as two independent z-source inverters. In SZSN-DIDOI, DC inputs form a common DC bus (capacitors of z-source network), and outputs are feed via this DC bus. Therefore, the power can be transferred from inputs to both outputs. However in SZSN-DIDOI, if one of DC inputs disconnect, none of the outputs can continue its operation [10].

8 Simulation and Experimental Results

The proposed inverter was simulated and a prototype of it was also built and controlled by a digital signal processor. Two similar resistance loads with LC filters were connected to outputs of the proposed inverter. Simulation and experimental parameters are listed in Table 4.

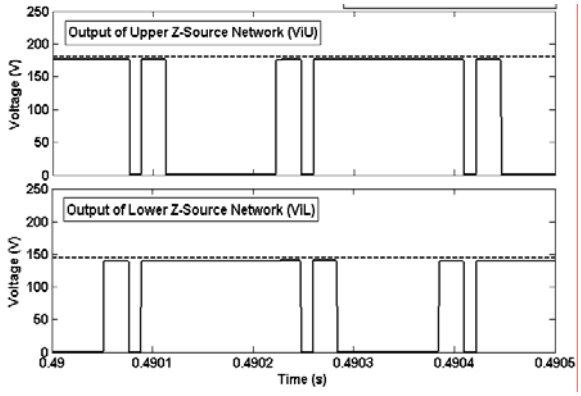
For the desired gains in Table 4 (G_U=2.15, G_L=1.85), B_U and B_L are determined using Table 3 as 4.96 and 4.01, respectively. Fig. 10 shows the output voltages of z-source networks V_{iU} and V_{iL} as 175V and 140V respectively which are slightly less than expected values from equations (1) and (2), (178 V and 144V). This is due to voltage drop across D_U and D_L diodes. Fig. 11 shows the result of the capacitor voltages equal to 105V and 88V (less than expected values of 108V and 90V). The line voltage and phase voltage of the proposed converter are shown in Fig. 12 and Fig. 13, respectively. It can be seen that both outputs have expected frequencies. The load currents are shown in Fig. 14. It can be seen that the load currents have nearly sinusoidal waveforms.

Table 4 Simulation and experimental parameters.

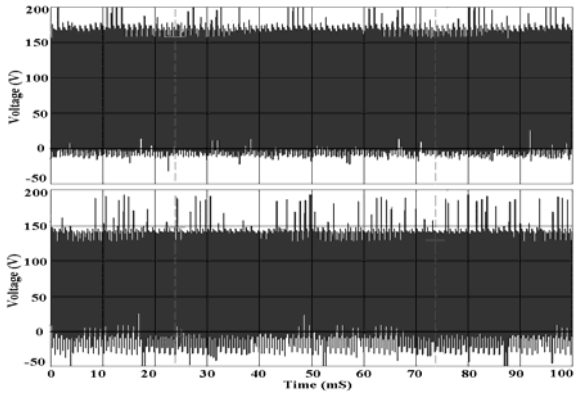
Parameter	Value
V_{oU}	36 V
V_{oL}	36 V
L_1 & L_2	4 mH
C_1 & C_2	2 mF
Switching Frequency	3 kH
G_U	2.15
G_L	1.85
F_U	25 Hz
F_L	50 Hz
R_{load}	5.6 Ohm
L_f	4 mH
C_f	20 uF

9 Conclusion

In this paper a novel nine-switch inverter was presented with two inputs and two outputs. The proposed inverter is composed of two z-source networks and a modified nine-switch inverter. The proposed inverter was compared with single z-source network dual-input dual-output inverter (SZSN-DIDOI) which has already been presented by the authors. Furthermore, a special control strategy based on voltage gains was presented to determine the type and time intervals of the switching vectors. Also a carrier-based PWM modulation was proposed for both the proposed inverter (DZSN-DIDOI) and SZSN-DIDOI. Simulation and experimental results verified performance and validity of the proposed inverter.

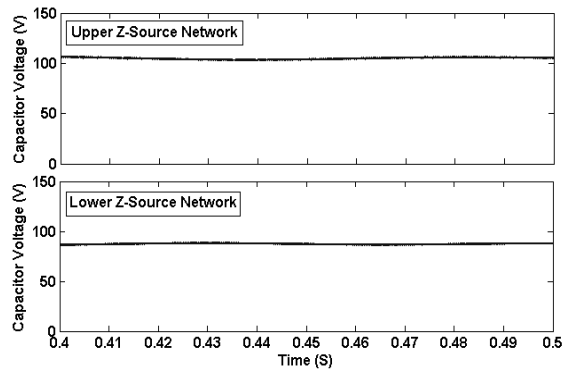


a) Simulation

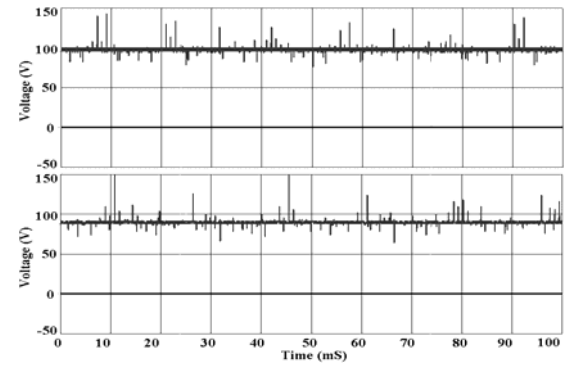


b) Experimental

Fig. 10 Outputs voltage of z-source networks (V_{iU} and V_{iL}).

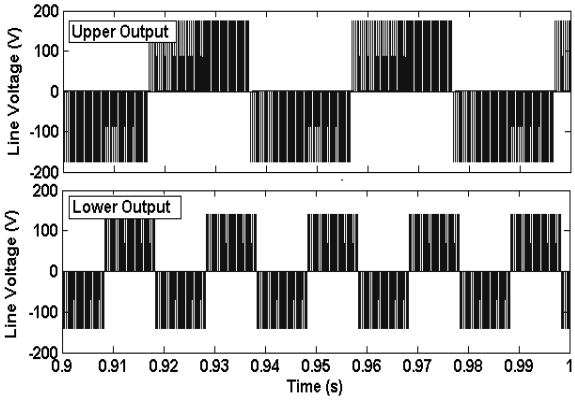


a) Simulation

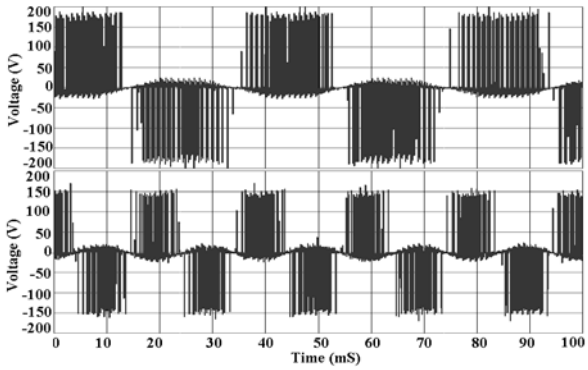


b) Experimental

Fig. 11 Capacitors voltage of z-source networks.

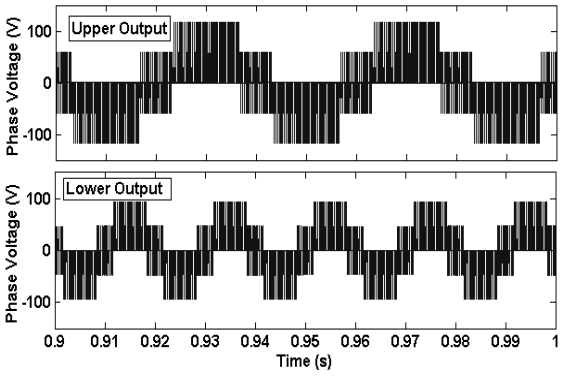


a) Simulation

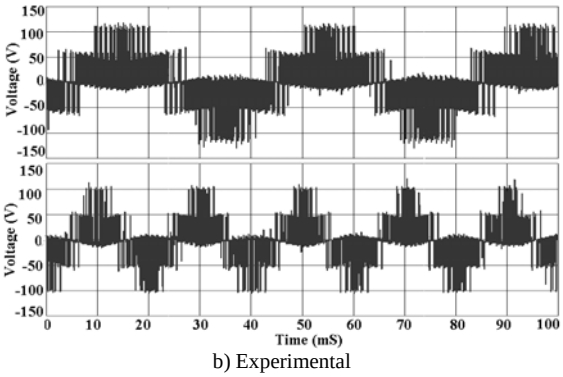


b) Experimental

Fig. 12 Line-line voltages of the proposed inverter.

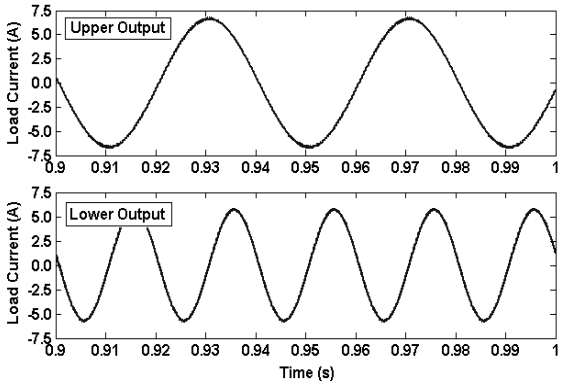


a) Simulation

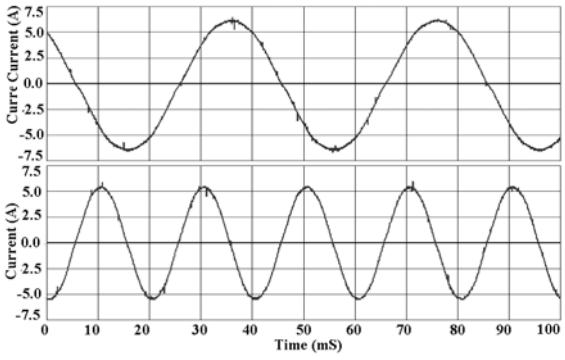


b) Experimental

Fig. 13 Phase voltage of the proposed inverter.



a) Simulation



b) Experimental

Fig. 14 Load currents of proposed inverter.

References

[1] Bojoi R., Tenconi A., Farina F. and Profumo F., "Dual-source fed multiphase induction motor drive for fuel cell vehicles: topology and control," *IEEE Power Electronics Specialists Conference (PESC'2005)*, pp. 2676-2683, 2005.

[2] Giraud F., Salameh Z. M., "Steady-State Performance of a Grid-Connected Rooftop Hybrid Wind–Photovoltaic Power System with Battery Storage," *IEEE Transactions on Energy Conversion*, Vol. 16, No. 1, pp. 1-7, 2001.

[3] Peng F. Z., "Z-Source Inverter," *IEEE Transactions on Industry Applications*, Vol. 39, No. 2, pp. 504-510, 2003.

[4] Gajanayake C. J., Vilathgamuwa D. M. and Loh P. C., "Development of a Comprehensive Model and a Multiloop Controller for Z-Source Inverter DG Systems," *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 4, pp. 2352-2359, 2007.

[5] Peng F. Z., Shen M. and Holland K., "Application of Z-Source Inverter for Traction Drive of Fuel Cell—Battery Hybrid Electric Vehicles," *IEEE Transactions on Power Electronics*, Vol. 22, No. 3, pp.1054-1061, 2007.

[6] Kominami T. and Fujimoto Y., "A Novel Nine-Switch Inverter for Independent Control of Two Three-phase Loads," *IEEE Industry Applications Society Annual Conference (IAS)*, pp. 2346-2350, 2007.

[7] Liu C., Wu B., Zargari N. and Xu D., "A Novel Three-phase Three-leg AC/AC Converter Using Nine IGBTs," *IEEE Transactions on Power Electronic*, Vol. 24, No. 5, pp. 1151-1160, 2009.

[8] Liu C., Wu B., Zargari N. and Xu D., "A novel nine-switch PWM rectifier-inverter topology for three-phase UPS applications," *Journal of European Power Electronics (EPE)*, Vol. 19, No. 2, pp. 1-10, 2009.

[9] Dehghan S. M., Mohamadian M. and Yazdian A., Ashrafzadeh F., "Space Vectors Modulation for Nine-Switch Converters," *IEEE Transactions on Power Electronics*, Vol. 25, No. 6, pp. 1488-1496, 2010.

[10] Dehghan S. M., Mohamadian M. and Yazdian A., Ashrafzadeh F., "Dual-Input Dual-Output Z-source Inverter," *IEEE Transactions on Power Electronics*, Vol. 25, No. 2, pp. 360-368, 2010.

[11] Loh P. C., Lim S. W., Gao F. and Blaabjerg F., "Three-Level Z-Source Inverters Using a Single LC Impedance Network," *IEEE Transaction on Power Electronics*, Vol. 22, No. 2, pp. 706-711, 2007.

[12] Tran Q.-V., Chun T.-W., Ahn J.-R. and Lee H.-H., "Algorithms for Controlling Both the DC Boost and AC Output Voltage of Z-Source Inverter," *IEEE Transactions on Industrial Electronics*, Vol. 54, No. 5, pp. 2745-2750, 2007.

[13] Peng F. Z., Shen M. and Qian Z., "Maximum Boost Control of the Z-Source Inverter," *IEEE Transactions on Power Electronics*, Vol. 20, No. 4, pp. 833-838, 2005.

[14] Thangaprakash S. and Krishnan A., "Implementation and Critical Investigation on Modulation Schemes of Three Phase Impedance Source Inverter," *Iranian Journal of Electrical & Electronic Engineering*, Vol. 6, No. 2, pp. 84-92, June 2010.

Seyed Mohammad Dehghan received the B.S. degree in Electrical Engineering from Islamic Azad University, Yazd, Iran, in 2003 and the M.S. and PhD degrees in Electrical Engineering from Tarbiat Modares University, Tehran, Iran, in 2005 and 2010, respectively. From November 2009 to April 2010, he was a Visiting Student with the Technical University of Denmark, Lyngby, Denmark. Since May 2010, he has been with Faratavan Automation Company, Tehran, Iran. His research interests include inverters, PWM rectifier, motor drives, inverter-based DGs, hybrid electric vehicles and FACTS.

Mustafa Mohamadian received the B.S. degree in Electrical Engineering from the AmirKabir University of Technology, Tehran, Iran, in 1989, the M.S. degree in Electrical Engineering from Tehran University, Tehran, Iran, in 1992 and the Ph.D. degree in Electrical Engineering, specializing in power electronics and motor drives, from the University of Calgary, Calgary, Canada in 1997. Since 2005, he has been with the Department of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran, as an Assistant Professor. His research interests include modeling, analysis, design, and control of power electronic converters/systems and motor drives., as well as embedded software development for power electronics and electric drives using microcontrollers and DSPs.

Ali Yazdian was born in Tehran, Iran. He received the B.Sc degree in Electrical Engineering from the Sharif University of Technology in 1989 and the M.Eng (Hons) and Ph.D. degrees in Electrical Engineering from the University of Wollongong, Australia, in 1995 and 1999, respectively. He is currently an Assistance Professor with the Department of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran. His research interests include FACTS, power quality, power system protection and information security.

Amir Hossien Rajaei received the B.S. degree in Electrical Engineering from Shiraz University, Shiraz, Iran, in 2006 and the M.S. degree in Electrical Engineering from Tarbiat Modares University, Tehran, Iran, in 2009. He is currently working toward the PhD degree with department of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran. His research interests include power converters, motor drives and inverter-based DGs.

Hossein Zahedi Abdolhadi was born in Kashan, Iran, in 1985. He received the B.S. degree in Electrical Engineering from the University of Kashan, Kashan, Iran, in 2007 and the M.S. degree in Electrical Engineering from Tarbiat Modares University, Tehran, Iran, in 2010. Since 2010, he has been with the Department of Electrical Engineering, Badrood Branch, Islamic Azad University, Badrood, Iran. His research interests include power converters and motor drivers as well as control of power electronics and electric drives using microcontrollers and DSPs.