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Research Paper

Low Voltage FVF Current Mirror With High Bandwidth and Low Input Impedance

N. Raj*(C.A.)

Abstract: The performance of any system is decided by the circuit configurations used in its implementation. Current mirror is one of those circuit configurations which are widely used in analog system designs. The performance of current mirror is decided by its parameters which include large operating range, wide bandwidth along with very low input and very high output resistances. In this paper, a low voltage flipped voltage follower based current mirror is presented. The structure flipped voltage follower is initially modified using a feedback path which results in the low impedance node which when considered as input in the proposed current mirror results in an extremely low value of input resistance. Compared to conventional flipped voltage follower based current mirror design the proposed design works well with minimum error in microamperes range with extended bandwidth without affecting its output resistance. The input resistance gets scaled down to 17 ohms from 840 ohms whereas bandwidth gets almost doubled approximately to 4.5GHz from 2.4GHz. The power dissipation ranges in microwatts. The simulations are supported with mathematical analysis. The complete analysis is done in HSpice using MOS models of 0.18-micron technology at a dual supply voltage, ±0.5V.

Keywords: Current Mirror, Flipped Voltage Follower, Input Resistance, Output Resistance, Bandwidth.

1 Introduction

CURRENT mirror is one of the fundamental blocks of any analog circuits which is extensively used in various purposes like for biasing in amplifiers, as active load, in current amplification, filtering, level shifter, etc. [1]. The current mirror generates the output as a function of input in the form of current. The parameters which decide its performance include operating range, bandwidth, input, and output resistances where other than input resistance all should be of high value. A lot many current mirror designs have been reported to fulfill the ideal requirements but unfortunately, all cannot be achieved at the same time due to various reasons. The utmost problem faced is the threshold voltage of MOS which is defined as, a minimum voltage required to turn on the device. In literature, some solutions to this have been presented [2] and based on these solutions few recent current mirror topologies can be found in [3-11]. Mainly the problem arises when the threshold of MOS becomes higher than the supply voltage. Few solutions include subthreshold operation, forward bias bulk source potential, low threshold MOS devices, etc. The alternative solution uses special structures of MOS, namely: floating and quasi floating, bulk-driven, and bulk-driven floating and quasi-floating gate MOS [2]. The goal gets fulfilled at the cost of special fabrication steps. In this paper, a low voltage topology is used for the current mirror design named Flipped Voltage Follower (FVF) [12] whose main advantage is in terms of low impedance node. The FVF structure is basically an improved common Drain configuration. Based on FVF, a few recent articles on low voltage current mirror circuits can be found in [13-21]. In this paper, the conventional FVF structure is modified, and based on this modified FVF, a current mirror is proposed. The proposed FVF current mirror has a wide operating range, gigahertz range bandwidth

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* The author is with the Department of Electronics & Communication Engineering, LNM Institute of Information Technology, Jaipur, India.
E-mail: nikhil.raj@lnmiit.ac.in.
Corresponding Author: N. Raj.
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and low input resistance (in tens of ohms) and high output resistance (in hundreds of kilo-ohms).

The paper is divided in five sections as follows. Section 2 briefs about the FVF and modified FVF structure. In Sections 3, the proposed FVF current mirror is discussed in detail. The HSpice simulations are shown in Section 4 and the conclusion is in Section 5.

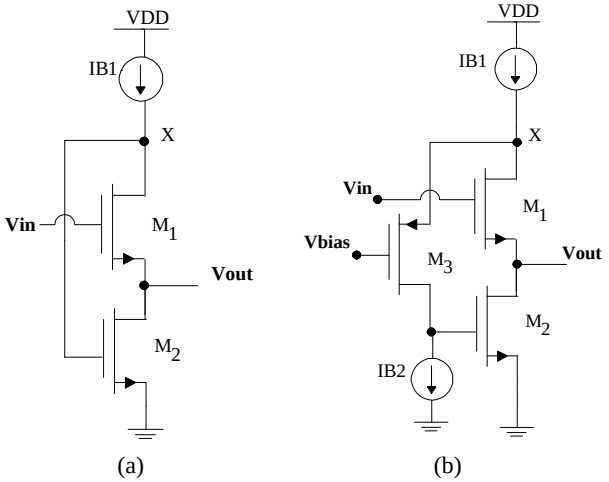
2 Flipped Voltage Follower

Among the basic MOS configurations, common Drain is commonly used as a voltage follower whose output tracks the input voltage with a DC level shift by one gate-source voltage drop. Being a basic block of analog circuits, designers keep on struggling to its low voltage operation with improved parameters. An ideal voltage follower should have high input and relatively low output resistance, high bandwidth and large swing. So, to overcome the drawbacks associated with common Drain configuration, an improved low voltage structure reported in the literature is shown in Fig. 1(a). The structure is named as flipped voltage follower whose advantage is in terms of low output resistance. The structure is basically a cascode stage with a shunt feedback due to which the output node experiences a low resistance $1/gm_2gm_1r_{01}$ where g_{mi} and r_{0i} denote the transconductance and output resistance of related transistor. Other features include high current sinking, extended bandwidth and low power [12]. In this paper, the modified design of FVF is presented as shown in Fig. 1(b). The modified design uses the PMOS in feedback path labeled as M_3. Performing the analysis, it is found that the modified FVF offers further reduced output impedance. Also, it enhances the frequency response of FVF.

3 Proposed Current Mirror

The FVF based current mirror design is shown in Fig. 2(a) which consists of four NMOS (M_1-M_4) where the input signal is fed to drain of M_3 and output is taken from the drain of M_4. Here MOS M_3 and current source I_{B1} forms a negative feedback. Since the drain current of M_3 remain constant, the change in input (I_{in}) is sensed by M_1 which produces subsequent change in its V_{GS} thus modulates the output current (I_{out}). The applied voltage V_{DD} ensures the NMOS M_3 and M_4 in saturation. The FVF current mirror's input and output resistances range in ohms and kilo-ohms, respectively.

In the proposed FVF current mirror, the changes made are in the feedback path by including an extra MOS M_5 as shown in Fig. 2(b). This MOS M_5 is biased in the saturation region which helped in reducing the node impedance by a scaling factor of ($g_{m5}r_{05}$). The effective input resistance of the proposed current mirror decreases and turns out to be in tens of ohms. Also, the changes made helped in improving the bandwidth without affecting its other parameters.

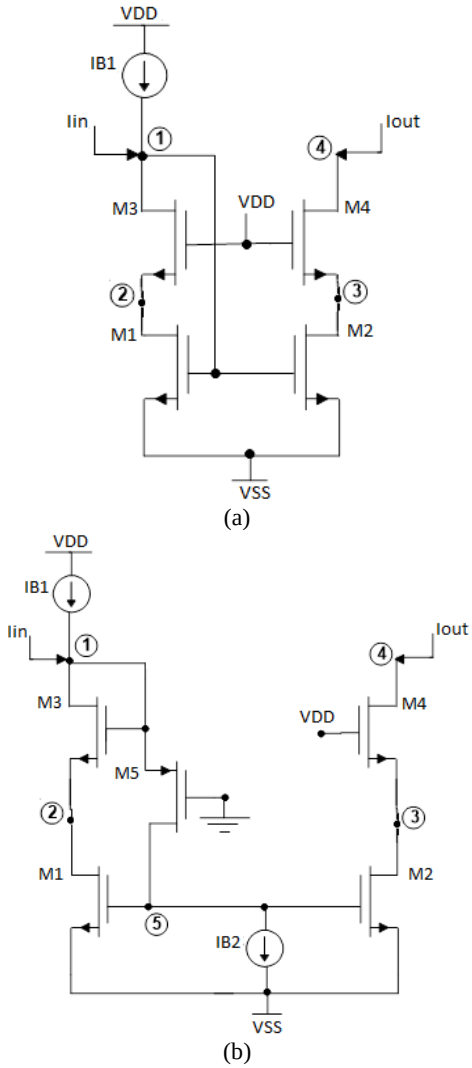


(a) (b)

Fig. 1 a) Flipped voltage follower (FVF) and b) Modified flipped voltage follower (FVF).

3.1 Small Signal Analysis

The small-signal analysis is carried in terms of input and output resistances and bandwidth. During analysis



(a) (b)

Fig. 2 a) Conventional FVF current mirror and b) Proposed FVF current mirror.

the symbols used matches to Spice model parameter of MOS transistors.

3.1.1 Input Resistance

The small-signal model for input resistance calculation ($R_{in,prop.}$) of the proposed FVF current mirror is shown in Fig. 3. Here R_1 and R_2 are the impedances of current source IB1 and IB2 respectively.

At node 1

$$i_{in} = g_{m3}V_{12} + \frac{V_1 - V_2}{r_{03}} + g_{m5}V_1 + \frac{V_1 - V_5}{r_{05}} + \frac{V_1}{R_1} \tag{1}$$

Since $g_m r_0 \gg 1$

$$i_{in} = \left(g_{m3} + g_{m5} + \frac{1}{R_1} \right) V_1 - g_{m3}V_2 - \frac{V_5}{r_{05}} \tag{2}$$

Similarly, at node 5

$$V_5 = g_{m5}\left(\frac{r_{05}}{R_2} \right) V_1 \tag{3}$$

and at node 2

$$V_2 = \frac{r_{01}}{1 + g_{m3}r_{01}} \left(g_{m3}V_1 - g_{m1}V_5 \right) \tag{4}$$

From (2)-(4)

$$i_{in} = \left(\frac{1}{R_1} + g_{m1}g_{m5}\left(\frac{r_{05}}{R_2} \right) \right) V_1 \tag{5}$$

For ideal current source $R_1 = R_2 = \infty$

$$i_{in} \approx g_{m1}g_{m5}r_{05}V_1 \tag{6}$$

$$R_{in,prop.} \approx \frac{1}{g_{m1}g_{m5}r_{05}} \tag{7}$$

whereas for conventional FVF current mirror, it is given as

$$R_{in,conv.} \approx \frac{1}{g_{m1}} \tag{8}$$

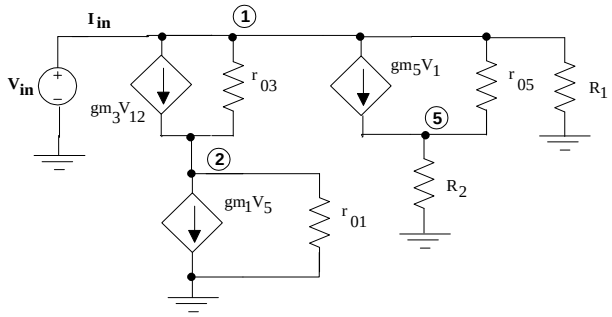


Fig. 3 Small-signal model for input resistance calculation.

Comparing (7) with (8), a scaling factor of ($g_{m5}r_{05}$) is observed in the input resistance of proposed circuit. Considering M5 working in saturation, the factor ($g_{m5}r_{05}$) helps to reduce input resistance to the minimum value.

3.1.2 Output Resistance

The small-signal model for output resistance calculation ($R_{out,prop.}$) of the proposed current mirror is shown in Fig. 4.

At node 4

$$i_{out} = -g_{m4}V_3 + \frac{V_4 - V_3}{r_{04}} \tag{9}$$

Since $g_m r_0 \gg 1$

$$i_{out} = -g_{m4}V_3 + \frac{V_4}{r_{04}} \tag{10}$$

At node 3

$$V_3 = i_{out}r_{02} \tag{11}$$

From (10) and (11)

$$R_{out} = \frac{V_4}{i_{out}} = \left(1 + g_{m4}r_{02} \right) r_{04} \tag{12}$$

$$R_{out,prop.} \approx \left(g_{m4}r_{04} \right) r_{02} \tag{13}$$

whereas for conventional FVF current mirror, it is given as

$$R_{out,conv.} \approx \left(g_{m4}r_{04} \right) r_{02} \tag{14}$$

Here comparing (13) with (14), no change is observed since the output structure remains the same. However, resistance can be enhanced by using topologies like regulated and super cascode at the cost of increased power dissipation.

3.1.3 Frequency Response

The small-signal model for bandwidth calculation of

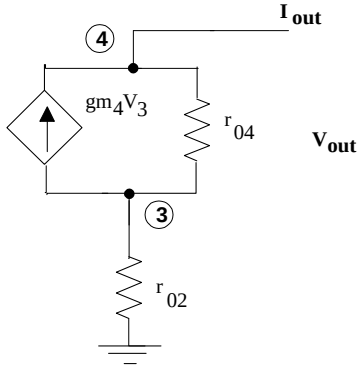


Fig. 4 Small-signal model for output resistance calculation.

the proposed current mirror is shown in Fig. 5. Here the output conductance is neglected, and also the C_{gd} effects in comparison to C_{gs} for saturation mode MOS transistors are neglected.

At node 4

$$i_{out} = -g_{m4}V_3 \tag{15}$$

At node 3

$$V_3 = -\frac{g_{m2}}{g_{m4}+sC_{gs4}}V_5 \tag{16}$$

At node 5

$$V_5 = \frac{g_{m5}}{s\left(C_{gs1}+C_{gs2}\right)}V_1 \tag{17}$$

From (15)-(17)

$$i_{out} = \frac{g_{m4}g_{m2}g_{m5}}{\left(g_{m4}+sC_{gs4}\right)s\left(C_{gs1}+C_{gs2}\right)}V_1 \tag{18}$$

At node 1

$$i_{in} = g_{m3}V_{12} + sC_{gs3}V_{12} + g_{m5}V_1 + sC_{gs5}V_1 \tag{19}$$

At node 2

$$g_{m3}V_{12} + sC_{gs3}V_{12} = g_{m1}V_5 \tag{20}$$

From (17)-(20)

$$i_{in} = \frac{g_{m1}g_{m5} + s\left(C_{gs1}+C_{gs2}\right)\left(g_{m5}+sC_{gs5}\right)}{s\left(C_{gs1}+C_{gs2}\right)}V_1 \tag{21}$$

From (18) and (21)

$$A_I = \frac{i_{out}}{i_{in}}$$

$$= \frac{g_{m4}g_{m2}g_{m5}}{\left(g_{m4}+sC_{gs4}\right)\left(g_{m1}g_{m5}+s\left(C_{gs1}+C_{gs2}\right)\left(g_{m5}+sC_{gs5}\right)\right)} \tag{22}$$

From (22), it can be observed that it is a 3rd order equation which on solving for roots results in one real and two complex poles as

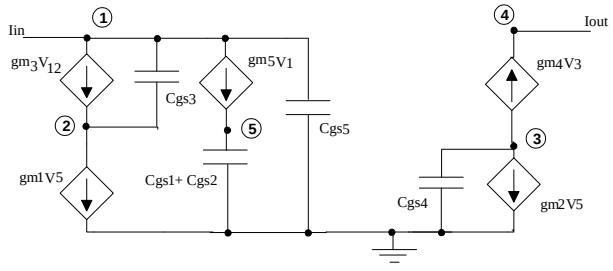


Fig. 5 Small-signal model for bandwidth calculation.

$$P_1 = -\frac{g_{m4}}{C_{gs4}} \tag{23}$$

$$P_{2,3} = -\frac{g_{m5}}{2C_{gs5}} \pm \frac{1}{2}\sqrt{\frac{g_{m5}}{C_{gs5}}}\sqrt{\frac{g_{m5}}{C_{gs5}} - \frac{4g_{m1}}{\left(C_{gs1}+C_{gs2}\right)}} \tag{24}$$

Here, the bandwidth of the proposed current mirror is decided by the dominant pole P_1 whereas for conventional FVF current mirror has the bandwidth given by

$$\omega_{n,conv.} = \sqrt{\frac{g_{m2}g_{m4}}{\left(C_{gs1}+C_{gs2}\right)C_{gs4}}} \tag{25}$$

As seen from (23) and (25), the proposed structure has higher bandwidth without consuming much power.

4 Simulation Results

The conventional and proposed FVF current mirrors of Fig. 2, is simulated in HSpice using MOS models of UMC in 0.18-micron technology at ±0.5V supply. The MOS width and length with other assumed parameters during circuit simulations are listed in Table 1.

The input bias current is set to 65 µA ensuring a lower offset in the circuit. The current transfer characteristics of conventional and proposed current mirror ranging from 0 to 500 µA are shown in Fig. 6 and the current copying error as percentage is shown in Fig. 7. As seen the error in the proposed FVF current mirror circuit is much lesser than its conventional counterpart thus providing better accuracy which is much lesser than unity. The output characteristic is in Fig. 8 where for the proposed circuit the output current has a lower offset.

Table 1 W and L of MOS used in the conventional and proposed FVF CM.

Transistors	W [µm]	L [µm]	Transistors	W [µm]	L [µm]
M1	25	0.24	M4	5	0.24
M2	25	0.24	M5	0.24	0.24
M3	5	0.24			
Supply = ±0.5 V, IB1 = IB2 = 1 µA					

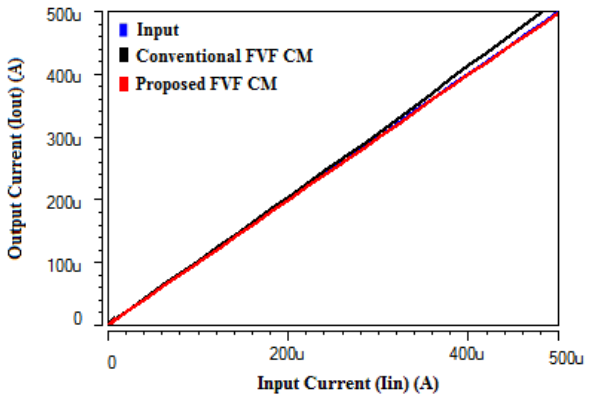


Fig. 6 Current transfer characteristics.

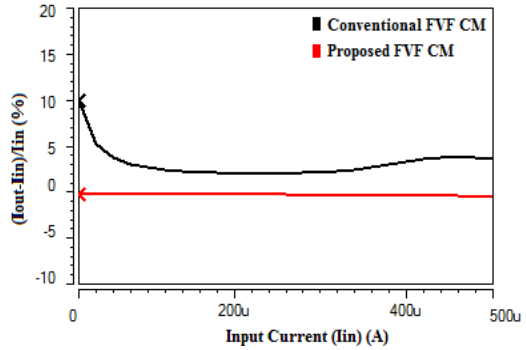


Fig. 7 Error in current transfer characteristics.

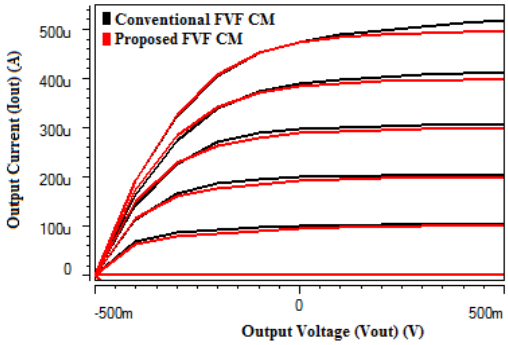


Fig. 8 Output characteristics.

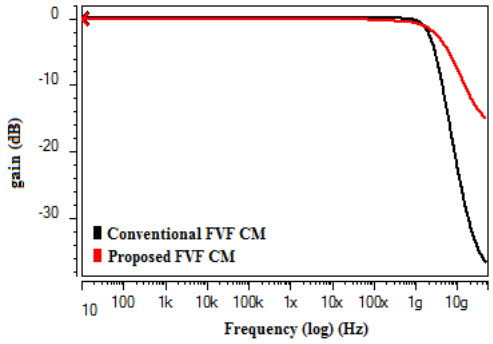


Fig. 9 Frequency responses.

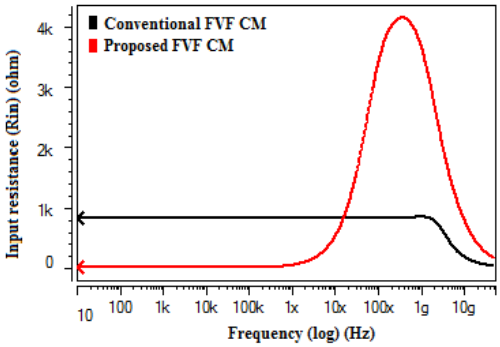


Fig. 10 Input resistances.

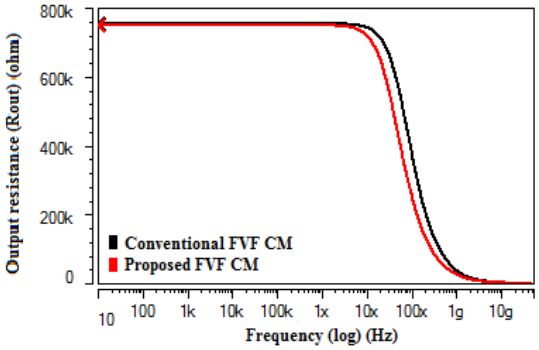


Fig. 11 Output resistances.

Table 2 Current matching error and Bandwidth variations at different process corners.

Input current [uA]	% Current transfer error ratio for			Frequency [Hz]	Gain [dB] for		
	Slow corner at 85°C	Typical corner at 27°C	Fast corner at –40°C		Slow corner at 85°C	Typical corner at 27°C	Fast corner at –40°C
20	-0.33	-0.30	-0.28	10	-0.03	-0.03	-0.02
60	-0.33	-0.29	-0.28	100	-0.03	-0.03	-0.02
100	-0.34	-0.29	-0.27	10K	-0.03	-0.03	-0.02
140	-0.35	-0.29	-0.27	100K	-0.03	-0.03	-0.02
180	-0.36	-0.30	-0.27	100M	-0.28	-0.24	-0.20
220	-0.38	-0.31	-0.27	1G	-0.92	-0.69	-0.54
260	-0.41	-0.32	-0.27	2G	-1.92	-1.41	-1.03
300	-0.45	-0.33	-0.27	2.5G	-2.48	-1.85	-1.35
340	-0.51	-0.35	-0.27	3.1G	-3.19	-2.41	-1.78
380	-0.60	-0.38	-0.28	4G	-4.08	-3.12	-2.33
420	-0.74	-0.41	-0.29	5G	-5.14	-3.99	-3.03
460	-0.98	-0.46	-0.30	6.3G	-6.37	-5.04	-3.89
500	-1.27	-0.53	-0.32	10G	-9.12	-7.56	-6.08

The frequency response, input resistance, and output resistance plots are shown in Figs. 9 to 11, respectively.

In the proposed design, using MOS M5 the bandwidth gets increased to 4.5 GHz from 2.4 GHz which is almost twice compared to conventional design. Similarly, the input resistance gets scaled down to 17 ohms from 840 ohms. However, the output resistance does not get affected which here is 750 kΩ. The robustness of the proposed current mirror circuit against environmental variations is shown with the help of process corner analysis at different temperatures. The circuit is simulated on three different process corners, namely

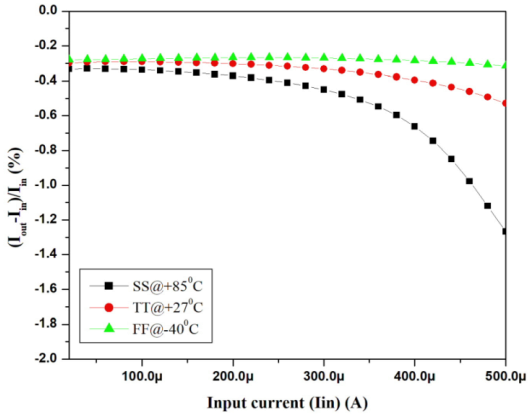


Fig. 12 Process corner analysis of current transfer error ratio of proposed current mirror.

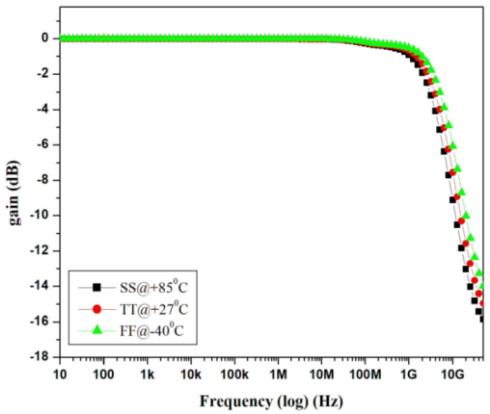


Fig. 13 Process corner analysis of Bandwidth of proposed current mirror.

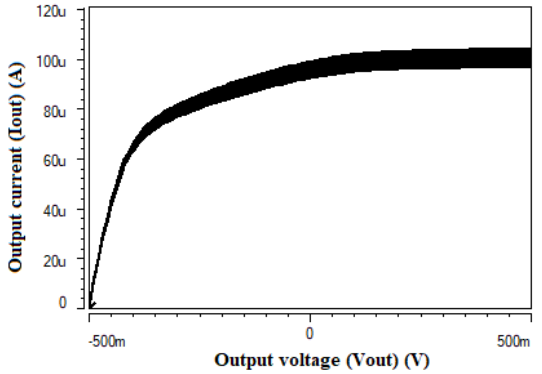


Fig. 14 Monte Carlo (100 runs) analysis of channel length mismatch on output characteristic of proposed current mirror at I_{in} = 100 µA.

Table 3 Comparison of parameters of the proposed current mirror with FVF current mirrors.

Parameters	[19]	[21]	Conventional FVF CM (Fig. 2(a))	Proposed FVF CM (Fig. 2(b))
Input current range [µA]	100	0-200	0-200	0-500
Current transfer error [%]	0.6	0.22	3.44	-0.409
Input resistance [Ω]	496	130	840	17
Output resistance [Ω]	1M	9.5G	754K	750K
Bandwidth [Hz]	181M	2.7G	2.4G	4.5G
Supply [V]	0.9	0.8	±0.5	±0.5
Power [µW]	150	79.33	110	140
Technology [µm]	0.18	0.18	UMC 0.18	UMC 0.18
FOM	0.6	94.4	0.8	647.2

Slow (at 85°C), Typical (at 27°C), and Fast (at –40°C).

The percentage in current transfer error ratio and bandwidth variations at the aforementioned process corners is tabulated in Table 2 and the corresponding plot is shown in Figs. 12 and 13, respectively.

As seen the current transfer error in percentage remains lesser than unity except for slow corner whereas the deviation in bandwidth is also less which ranges between 3.5 GHz to 5.5 GHz. Further analysis is carried in terms of MOS channel length mismatch on output characteristic through Monte Carlo simulations (100 runs). A 5% mismatch in channel length of MOS transistors is applied with the help of Gaussian distribution. From the plots, it can be observed that the proposed current mirror operates within an acceptable range in the whole design space.

The complete simulated HSpice simulations of conventional and proposed FVF current mirrors are shown in Table 3 and also it is compared with simulations of recently reported low power, FVF current mirrors.

5 Conclusion

A low voltage modified design of FVF structure and based on this a low voltage current mirror circuit has been presented in this paper. The parameters of current mirror improved were in terms of input resistance and bandwidth range. The input resistance gets scaled down to an extremely low value and bandwidth gets doubled by using modified FVF with a slight increase in power. The modified FVF uses the feedback which lowers the node impedance. However, this change does not affect the output resistance. In order to improve the output resistance, techniques like cascode, super cascode, etc. can be used. The complete analyses were done using MOS models of 0.18-micron technology at a supply voltage ±0.5 V. The proposed microwatt range current mirror with a low input resistance of 17 ohms and wide bandwidth of 4.5 GHz encourages its application for low power electronic devices.

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N. Raj received his M.Tech and Ph.D. degree in VLSI Design in 2010 and 2017, respectively from the National Institute of Technology, Kurukshetra, India. He has teaching and research experience in India as well abroad. Currently, he is working as an Assistant Professor in the Department of ECE at LNM Institute of Technology Jaipur, India. His research interest includes low power circuit design, current-mode circuits, etc.