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Simulation and Comparison of Twenty Five Level Diode Clamped & Cascaded H-Bridge Multilevel Inverter

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Abstract: This paper presents the comparative study of three phase twenty five level diode clamped and cascaded H-bridge multilevel inverters. The comparison is made in respect of requirement of devices, quality of output voltage and reduction of total harmonic distortion at the multilevel inverter terminals. In this work multicarrier sinusoidal pulse modulation control methods of Phase disposition (PD-PWM), phase opposition disposition (POD-PWM) and Alternative Phase Opposition Disposition (APOD-PWM) pulse width modulation control strategies are applied for both diode clamped and cascaded H-bridge multilevel inverters and compared its total harmonic distortion. The performance of both diode and cascaded H-bridge multilevel inverters is investigated and compared. Based on simulation results it is observed that the output voltage of the cascaded H-bridge multilevel inverters is better as compared to the diode clamped multilevel inverter. The proposed multilevel inverters are simulated using MATLAB/Simulink software.

Keywords: Diode Clamped Type Multilevel Inverter, Cascaded H-Bridge Multilevel Inverter, Phase Disposition Pulse Width Modulation (PD-PWM), Phase Opposition Disposition Pulse Width Modulation (POD-PWM), Alternative Phase Opposition Disposition Pulse Width Modulation (APOD-PWM), Total Harmonic Distortion, Twenty Five Level Inverter.

1 Introduction

RECENTLY, industrial application of multilevel inverter is becoming increasingly popular due to their valuable characteristics such as lower total harmonic distortion (THD), higher efficiency and lower switching voltage stress [1,2]. The multilevel inverter with more voltage levels exhibits better operational characteristics. Nevertheless, more voltage levels means increased number of power electronic switches in the circuit. As the number of power electronic switches increases, the inverter's cost increases proportionately. For high power application, multilevel inverters are widely used such as static VAr compensators, drives and active power filters. The advantages of multilevel inverters are good power quality, low switching losses and high voltage capability [3-6].

There are mainly three types of multilevel inverter structures used in industrial applications:

1. Diode clamped type inverter
2. Flying capacitors type inverter
3. Cascaded H-bridges inverter

Diode clamped and cascaded H-bridge multilevel inverters are very commonly used topology for motor drive and power quality improvement applications. In diode clamped inverter, each of three phase inverter sharing a common DC source and it is subdivided by using capacitor and the voltage across each capacitor is Vdc. The number of voltage levels in multilevel inverter can be increased by adding the additional capacitors, diodes and power devices. The clamping diodes are used to limit stress on the power device. The Clamping diodes and capacitor having same capacity per unit [7-11]. The main drawbacks of basic diode clamped

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multilevel inverter are unbalance voltage across each capacitor, complexity of circuit by increasing more number of levels, more number of clamping diodes with higher rating and dc voltage sources, it increased cost & size of the system. To overcome these problems cascaded H-bridge multilevel inverters are used. The cascaded H-bride inverter is simple in structure and reliable. It doesn't require clamped diodes and the number of dc voltage sources required is also low. The cascaded H-bride inverters requires separate dc source for each H-bridge. For m-levels output voltage, the single phase full bridge inverters required are (m-1)/2 [12-15].

The switching on and off the power devices in multilevel inverters is done using modulation control technique. The efficiency of multilevel inverter, switching stress on power devices and harmonic content in the output voltage of the multilevel inverter depends upon modulation technique used [16]. Different Pulse width modulation strategy has been developed for multilevel inverters in which mostly sinusoidal pulse width modulation (SPWM) method [17], space vector modulation (SVM) method and selective harmonic elimination (SHE) modulation techniques are used. In which the SVM method is more complicated and it requires more calculations [18-20]. The SHE method is required optimal switching angle for that it requires more accurate iterative procedure [21,22]. In SPWM method multi carrier wave signals are compared with reference signal, the obtained compared pulses are used to switching of inverter. In this paper SPWM control method is used.

From lower to higher voltage levels total harmonic distortion and components required is different for both cascaded H-bridge inverter. Many authors proposed only lower voltage levels but higher voltage levels not up to the mark. In this paper twenty five level diode and cascaded H-bridge multilevel inverter is simulated. The total harmonic distortion and its output voltage of the both multilevel inverter are compared. The sinusoidal PWM modulation control scheme of PD-PWM, POD-PWM & APOD-PWM is applied for switching of both the multilevel inverters and compared their modulation control strategies. Section 2 presents diode clamped multilevel inverter, Section 3 represents cascaded H-bridge multilevel inverter, section 4 presents the modulation control strategy, Section 5 gives the results and discussion, Finally section 6 gives Conclusions.

2 Twenty Five Level Diode Clamped Multilevel Inverter

The m-level diode clamped type inverter required (m-1) capacitors. Here instead of capacitor, dc voltage sources are used. In this 2(m-1) switching or power devices and (m-1) (m-2) clamping diodes are required to produce m-levels in the output phase voltage [6-9]. Fig. 1 shows the three phase twenty five level diode clamped type multilevel inverter. The R-phase, Y-phase & B-phase switches indicated by S1R, S2R, S3R … S48R, S1Y, S2Y, S3Y … S48Y and S1B, S2B, S3B … S48B. It consists of total twenty four dc voltage sources, V1R – V24R for R-phase, V1Y – V24Y for Y-phase, V1B-V24B for B-phase. Here the voltage across each dc voltage source is taken equal. Total 48 Power switch (IGBT) is used per phase, for three phase total 144 switches. The voltage stress across each power device is limited to Vdc/24 by using clamping diodes. It becomes total 576 clamping diodes are used. The neutral point n is considered as reference for output voltage representation in per phase as shown in Fig. 1. The output voltage and switching pattern of one phase leg or per phase of twenty five level diode clamped inverter is shown in Table 1. When the switches S1R to S24R is turned on the output voltage is V1. The switches S2 to S24 and S25 turned on output voltage is V2 and so on. Fig. 2 shows the simulink diagram of twenty five level diode clamped inverter.

The R-phase switches S1R – S48R, Y-phase switches S1Y – S48Y, B-phase switches are S1B – S48B. Here total twenty four complementary switches (S1, S25), (S2, S26) … (S24, S48) are used. The switches S1 – S24 are upper (positive) switches and switch S25 – S48 are lower (negative) switches per phase. Each Phase of the three-phase twenty five level diode clamped multi-level inverter has 48 bi-directional switches as shown in Fig. 1. The gate switching of each power (IGBT switch) device is obtained from proposed modulation control methods.

3 Twenty Five Level Cascaded H-Bridge Multilevel Inverter

The three phase twenty five level cascaded H-bridge multilevel inverter circuit diagram is shown in Fig. 2. The 'm' number of output phase voltage levels is obtained using the formula m = 2s+1. Where 's' is the number of dc sources [12-15]. In the same way the 'n' individual cascaded H-bridge module produces 'm' number of output phase voltage levels using the formula m = 2n+1. The cumulative magnitude of output phase voltage of 'm' level cascaded H-bridge inverter is Vamt = Va1+Va2+Va3+…+Vam. The R-phase, Y-phase & B-phase switches indicated by S1R, S2R, S3R … S48R, S1Y, S2Y, S3Y … S48Y and S1B, S2B, S3B … S48B. It consists of per phase total twelve individual dc voltage sources from, V1R – V12R for R-phase, V1Y – V12Y for Y-phase, V1B – V12B for B-phase. In this paper the voltage across each dc voltage source is taken equal. The total 48 Power switches (IGBT) are used per phase, for three phase total 144 switches are used. The switching states and output voltage of one phase leg or per phase twenty five level cascaded H-bridge inverter is given in Table 2. In R-phase, when the switches S1R and S2R is turn on, the output voltage positive. When the switches S25R and S26R are turn on, the output voltage is negative. When the switches S1R, S25R or S2R, S26R are turned on, the output

Table 1 Switching states and output voltage of one phase leg of twenty five level diode clamped inverter.

ON position	OFF Position	Output Voltage (V)
S1R – S24R	S25 – S48	V1
S2 – S24, S25	S1, S26 – S48	V2
S3 – S24, S25, S26	S1, S2, S27 – S48	V3
S4 – S24, S25 – S27	S1 – S3, S28 – S48	V4
S5 – S24, S25 – S28	S1 – S4, S29 – S48	V5
S6 – S24, S25 – S29	S1 – S5, S30 – S48	V6
S7 – S24, S25 – S30	S1 – S6, S31 – S48	V7
S8 – S24, S25 – S31	S1 – S7, S32 – S48	V8
S9 – S24, S25 – S32	S1 – S8, S33 – S48	V9
S10 – S24, S25 – S33	S1 – S9, S34 – S48	V10
S11 – S24, S25 – S34	S1 – S10, S35 – S48	V11
S12 – S24, S25 – S35	S1 – S11, S36 – S48	V12
S13 – S24, S25 – S36	S1 – S12, S37 – S48	0
S14 – S24, S25 – S37	S1 – S13, S38 – S48	-V12
S15 – S24, S25 – S38	S1 – S14, S39 – S48	-V11
S16 – S24, S25 – S39	S1 – S15, S40 – S48	-V10
S17 – S24, S25 – S40	S1 – S16, S41 – S48	-V9
S18 – S24, S25 – S41	S1 – S17, S42 – S48	-V8
S19 – S24, S25 – S42	S1 – S18, S43 – S48	-V7
S20 – S24, S25 – S43	S1 – S19, S44 – S48	-V6
S21 – S24, S25 – S44	S1 – S20, S45 – S48	-V5
S22 – S24, S25 – S45	S1 – S21, S46 – S48	-V4
S23, S24, S25 – S46	S1 – S22, S47, S48	-V3
S24, S25 – S47	S1–S23, S48	-V2
S25 – S48	S1 – S24	V1

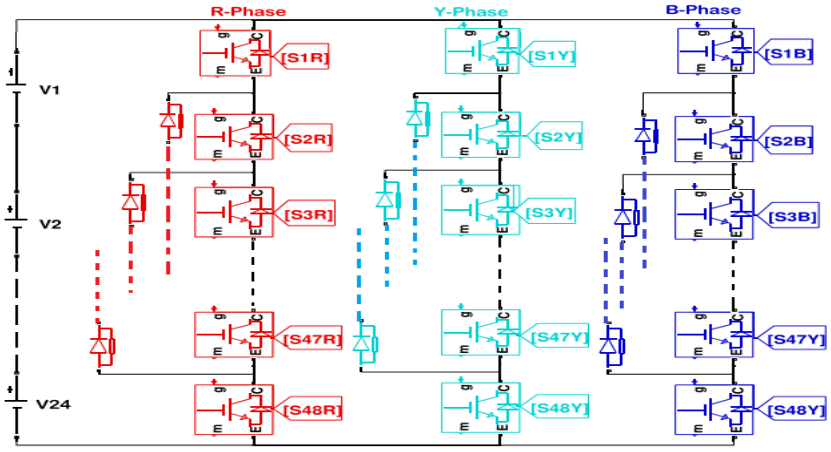


Fig. 1 Three phase twenty five level diode Clamped type multilevel inverter.

voltage is zero, for single H-bridge and it is same for all other H-bridges of R-phase, and also for Y-phase & B-phases as shown in Fig. 3. Its simulink diagram is shown in Fig. 4.

The operation of diode and cascaded H-bridge multilevel inverter is discussed in the sections 2 & 3. From the discussion it is observed that the both techniques required same number of power switches. But the clamping diodes requirement is eliminated and number of dc voltage sources required less in cascaded H-bridge inverter. The comparison of components requirements of both the inverter levels is given in Table 3. The simulation and switching technique of cascaded H-bridge inverter is very convenient compared to diode clamped inverter.

4 Modulation Control Strategy

In this paper level shifted methods of Phase disposition pulse width modulation (PDPWM), Phase opposite disposition pulse width modulation (PODPWM) and alternative Phase opposite disposition pulse width modulation (APODPWM) methods are used and compared. In level shifted SPWM control method several triangular carrier wave signals are compared with modulated reference sinusoidal signal. For m-level output, (m-1) carrier wave signals are required. The reference wave is constant magnitude and frequency, the carrier waves also having equal magnitude and level shifted. For generating the switching pulses the

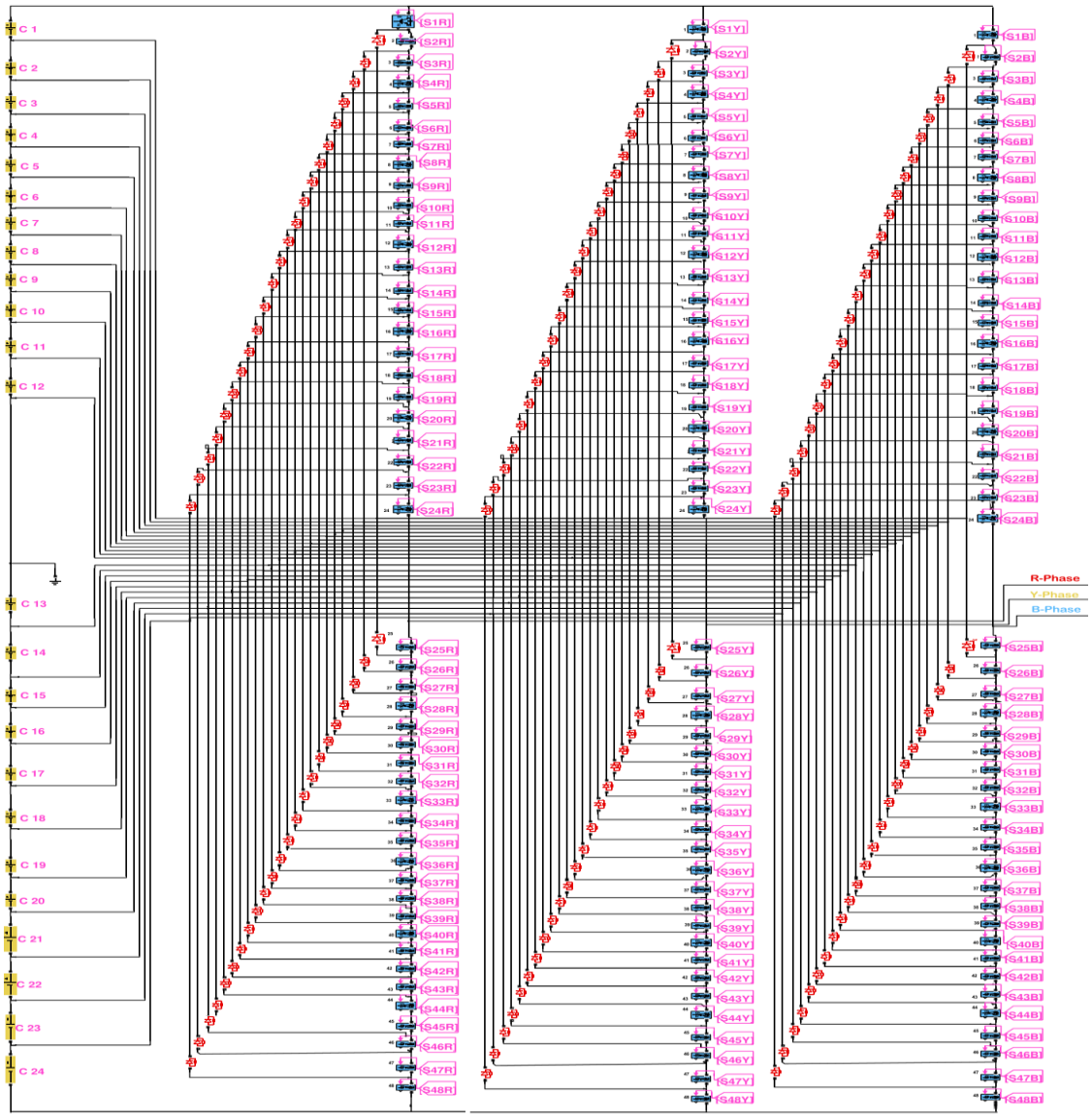


Fig. 2 Simulink model diagram of twenty five level diode clamped multilevel inverter.

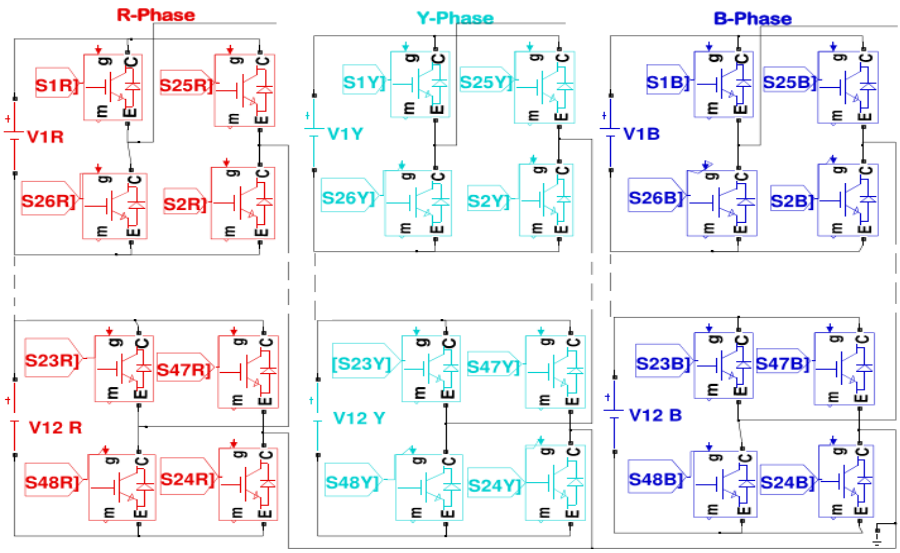


Fig. 3 Three phase twenty Five level cascaded H-bridge multilevel inverter.

Table 2 Switching states and output voltage of one phase leg of twenty five level cascaded H-bridge multilevel inverter.

ON position	OFF Position	Output Voltage
S1R – S24R	S25R – S48R	V12
S1R – S22R, S24, S48	S23R, S25R – S47R,	V11
S1R – S20R, S22R, S24R, S46R, S48R	S21R, S23R, S25R – S45R, S47R	V10
S1R – S18R, S20R, S22R, S24R, S44R, S46R, S48R	S19R, S21R, S23R, S25R – S43R, S45, S47R	V9
S1R – S16R, S18R, S20R, S22R, S24R, S42R, S44R, S46R, S48R	S17R, S19R, S21R, S23R, S25R – S41R,S43R,S45R, S47R	V8
S1R – S14R, S16R, S18R, S20R, S22R, S24R,S40R,S42R, S44R, S46R, S48R	S15, S17, S19R, S21R, S23R, S25R – S39R, S41R, S43R, S45, S47R	V7
S1R – S12R, S14,S16, S18, S20R, S22R, S24R, S38R, S40R, S42R,S44R, S46R, S48R	S13,S15, S17,S19R, S21R, S23R, S25R – S37R, S39R,S41R,S43R,S45R,S47R	V6
S1R – S10R, S12, S14,S16, S18, S20R, S22R, S24R, S36R,S38R, S40R, S42R,S44R, S46R, S48R	S11, S13,S15, S17,S19R, S21R, S23R, S25R – S35R, S37R, S39R, S41R, S43R,S45R,S47R	V5
S1R – S8R, S10R, S12,S14,S16, S18, S20R, S22R, S24R, S34R,S36R,S38R, S40R, S42R,S44R, S46R, S48R	S9,S11, S13,S15, S17,S19R, S21R, S23R, S25R – S33R, S35R, S37R, S39R, S41R, S43R,S45R,S47R	V4
S1R – S6R,S8R, S10R, S12,S14,S16, S18, S20R, S22R, S24R, S32R,S34R,S36R,S38R, S40R, S42R,S44R, S46R, S48R	S7,S9, S11, S13,S15, S17,S19R, S21R, S23R, S25R – S31R, S33R, S35R, S37R, S39R, S41R, S43R,S45R,S47R	V3
S1R – S4R, S6R, S8R, S10R,S12, S14,S16, S18, S20R, S22R, S24R, S30R, S32R,S34R,S36R,S38R, S40R, S42R,S44R, S46R, S48R	S5,S7,S9,S11,S13,S15,S17,S19R, S21R, S23R, S25R – S29R, S31, S33R, S35R, S37R, S39R, S41R, S43R,S45R,S47R	V2
S1R –S2R, S4R,S6R, S8R, S10R,S12, S14,S16, S18, S20R,S22R,S24R,S28R,S30R, S32R,S34R,S36R,S38R , S40R, S42R,S44R, S46R, S48R	S3R,S5R,S7R,S9R,S11R,S13,S15, S17,S19R, S21R, S23R, S25R – S27R, S29R,S31, S33R, S35R, S37R,S39R,S41R,S43R,S45R,S47R	V1
S2R, S4R, S6R, S8R, S10R, S12R, S14R, S16R, S18R, S20R, S22R, S24R, S26R, S28R, S30R, S32R, S34R, S36R, S38R, S40R, S42R, S44R, S46R, S48R	S1R, S3R, S5R, S7R, S9R, S11R, S13R, S15R, S17R, ,S19R, S21R, S23R, S25R , S27R, S29R, S31R, S33R, S35R, S37R, S39R, S41R, S43R, S45R, S47R	0
S2R, S4R, S6R, S8R, S10R, S12, S14, S16, S18, S20R, S22R, S26R, S28R, S30R, S32R, S34R, S36R, S38R, S40R, S42R ,S44R, S46R – S48R	S1R,S3R,S5R,S7R,S9R, S11R, S13,S15, S17,S19R, S21R, S23R – S25R , S27R, S29R,S31, S33R, S35R, S37R, S39R, S41R, S43R,S45R,S47R	-V1
S2R, S4R, S6R, S8R, S10R, S12R, S14R, S16, S18, S20R, S26R, S28R, S30R, S32R, S34R, S36R, S38R, S40R, S42R, S44R – S48R	S1R,S3R,S5R,S7R,S9R, S11R, S13,S15, S17,S19R, S21R – S25R , S27R, S29R,S31, S33R, S35R, S37R, S39R, S41R, S43R	-V2
S2R, S4R, S6R, S8R, S10R, S12R, S14R, S16R, S18R, S26, S28R, S30R, S32R,S34R,S36R,S38R, S40R, S42R–S48R	S1R,S3R,S5R,S7R,S9R, S11R, S13,S15, S17, S19R – S25R , S27R, S29R,S31, S33R, S35R, S37R, S39R, S41R	-V3
S2R,S4R, S6R, S8R, S10R,S12, S14,S16, S26, S28R, S30R, S32R,S34R,S36R,S38R, S40R – S48R	S1R,S3R,S5R,S7R,S9R,S11R, S13,S15,S17–S25R,S27R, 29R,S31,S33R,S35R,S37R, S39R	-V4
S2R,S4R, S6R, S8R, S10R,S12, S14, S26,S28R,S30R,S32R,S34R,S36R,S38R – S48R	S1R,S3R,S5R,S7R,S9R, S11R, S13, S15 – S25R , S27R, S29R,S31, S33R, S35R, S37R	-V5
S2R, S4R, S6R, S8R, S10R, S12R, S26R, S28R, S30R, S32R, S34R, S36R – S48R	S1R, S3R, S5R, S7R, S9R, S11R, S13R – S25R , S27R, S29R, S31R, S33R, S35R	-V6
S2R, S4R, S6R, S8R, S10R, S26R, S28R, S30R, S32R, S34R – S48R	S1R, S3R, S5R, S7R, S9R, S11R – S25R , S27R, S29R, S31, S33R	-V7
S2R, S4R, S6R, S8R, S26, S28R, S30R, S32R – S48R	S1R, S3R, S5R, S7R, S9R – S25R , S27R, S29R, S31R	-V8
S2R, S4R, S6R, S26, S28R, S30R – S48R	S1R, S3R, S5R, S7R – S25R , S27R, S29R	-V9
S2R, S4R, S26R, S28R – S48R	S1R, S3R, S5R – S25R, S27R	-V10
S2R, S26R – S48R	S1R, S3R – S25R	-V11
S25R – S48R	S1R – S24R	-V12

reference voltage is compared with the triangular carrier wave at every instant. In this paper for the development of twenty five level three phase inverter, the twenty four continuous carrier wave having switching frequency of 20 kHz and 40 kHz is compared with the three phase sinusoidal reference wave having switching frequency of 50Hz. In reference three phase wave, the R-phase indicated red color, Y-phase indicted yellow color B-phase is indicated by blue color. The switching of individual inverter, for example R-phase inverter switching the R-phase reference signal is compared with the twenty four carrier wave signals in the same way Y-phase and B-phase inverters.

4.1 Phase Disposition (PD-PWM) Pulse Width Modulation Method

The switching pulses of twenty five level diode

Table 3 Comparison of component requirement in diode clamped and cascaded H-bridge multilevel inverter per phase leg.

Type of inverter	Diode clamped multilevel inverter		Cascaded H-bridge multilevel inverter	
	twenty five level	Formula used	twenty five level	Formula used
DC sources	24	(m-1)	12	(m-1)/2
IGBT switches	48	2 (m-1)	48	2 (m-1)
Clamped diodes	76	(m-1)(m-2)	–	–

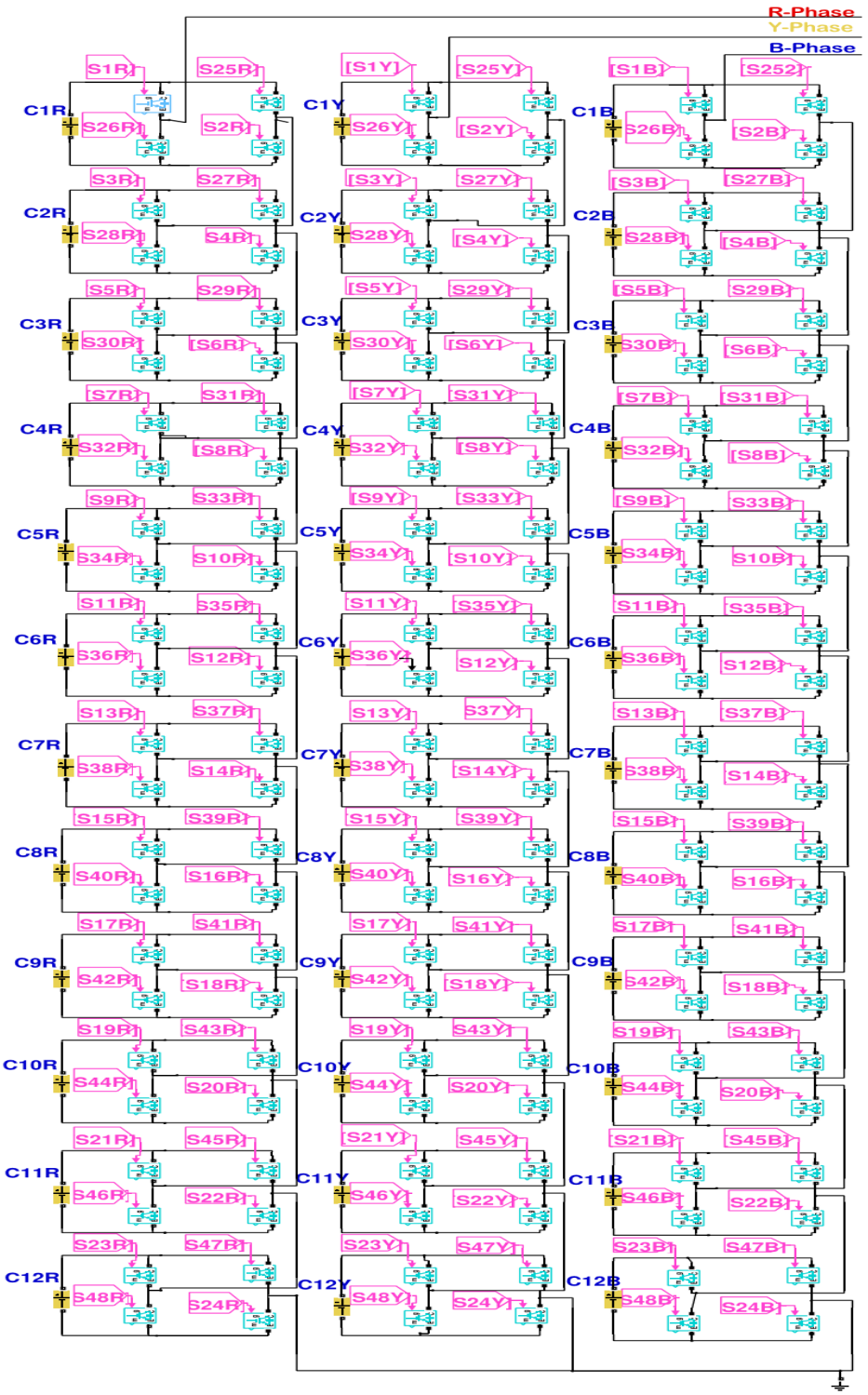


Fig. 4 Simulink model diagram of twenty five level cascaded H-bridge multilevel inverter.

clamped and cascaded H-bridge inverter is obtained from, level shifted phase disposition pulse width Modulation (PD-PWM) control strategy is shown in Fig. 5. Here the twenty four carrier wave signals are compared with three phase sinusoidal reference signal, the obtained compared signals are used for switching of the inverter. All carrier wave signals having equal maximum and minimum positions. The output voltage is positive all the cases, when the reference sinusoidal signal is greater than all upper carrier wave signals (above zero reference). The output voltage negative for all the cases, when the reference carrier wave signal is less than the all lower carrier wave signals (below zero reference).

4.2 Phase Opposition Disposition Pulse Width Modulation (POD-PWM) Method

The level shifted phase Opposition Disposition Pulse width modulation (POD-PWM) strategy is shown in Fig. 6. All carrier wave signals are having equal magnitude and shifted levels. The level difference between each carrier wave signal is 0.5. From the Fig. 6, it is observed that in POD-PWM method all carrier waves in positive cycle (above the zero reference) is in phase with each other, in negative cycle (below the zero reference) is 1800 out of phase as compared to positive cycle. Further it is noted that above zero reference is positive switching and below the zero reference is negative switching.

4.3 Alternative Phase Opposition Disposition Pulse Width Modulation (APOD-PWM) Method

The sinusoidal level shifted APOD-PWM method is shown in Fig. 7. In APOD-PWM method all the carrier waves signals are alternatively phase displaced by 1800 in their adjacent carrier wave signals. Here twenty four carrier wave signals are comparing with three phase sinusoidal reference signals, the obtained compared signals are used for switching of the inverter. The magnitude difference between each carrier wave is 0.5. The output voltage is positive for upper carrier waves switching (0 carrier wave level to 6 carrier wave level) and the output voltage is negative for lower carrier wave switching (0 carrier wave level to -6 carrier wave level) as shown in Fig. 7. The three phase wave form are phase displaced by 1200 from each other.

5 Results and Discussion

In this research paper the output voltages and total harmonic distortion of diode clamped & cascaded H-bridge multilevel inverter are compared. From the

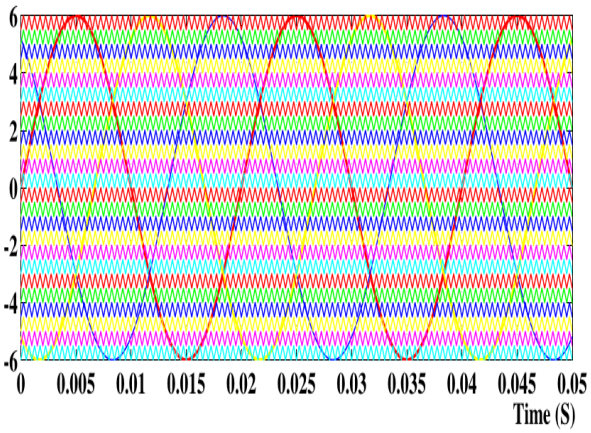


Fig. 5 PD-PWM method.

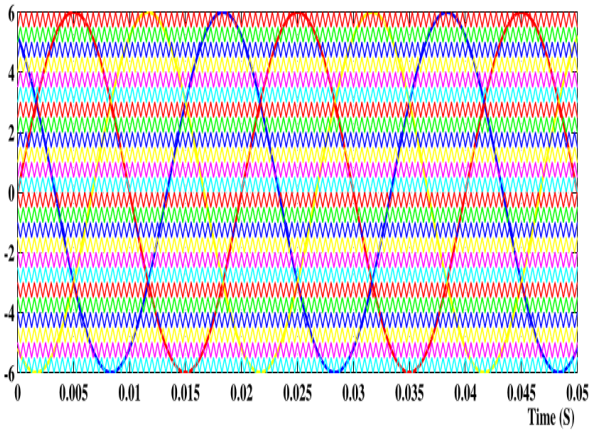


Fig. 6 POD-PWM method.

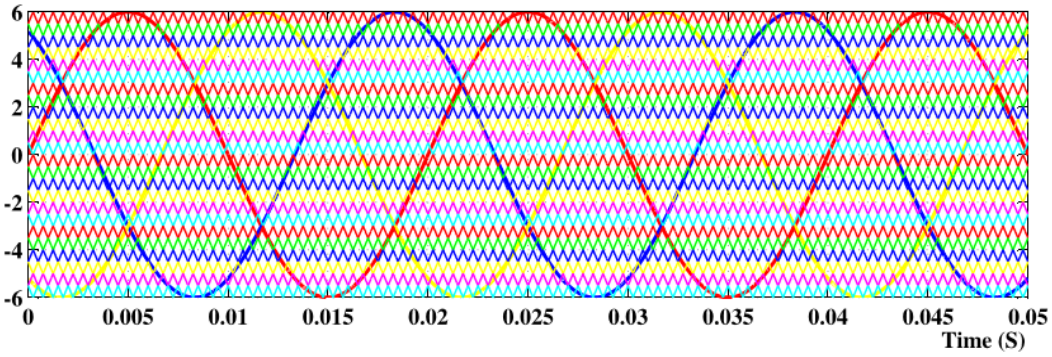


Fig. 7 APOD-PWM method.

simulation results it is observed that, by increasing the number of level, the output voltage of the cascaded H-bridge is more as compared to diode clamped multilevel inverter. The voltage across each dc voltage source is 100V for both multilevel inverters, the load résistance is 1.5Ω per phase and modulation index 'm' is taken as unity for both inverters. The IGBT values for the techniques are same. The clamped diodes used for diode clamped inverter all are having same values. The corresponding results are obtained using MATLAB/Simulink software. The R-Phase, Y-Phase, B-Phase are indicated by red, yellow and blue lines. For better comparison the simulation period considered as 0.1 sec for both the inverters.

5.1 Twenty Five Level Diode Clamped Multilevel Inverter

The three phase output voltage of twenty five level diode clamped multilevel inverter as shown in Fig. 8. The total magnitude of phase voltage output is 1000V. The output line voltage magnitude is 1732V. The three phase line & phase voltage output are shown in Figs. 8(a) and 8(b).

5.2 Twenty Five Level Cascaded H-Bridge Multilevel Inverter

The three Phase voltage output of twenty five level cascaded H-bridge multilevel inverter as shown in Fig. 9. The total phase voltage output magnitude is 1200V and its line voltage output is 2079V. Each switch is sharing equal amount of voltage. The three phase line and phase voltage output are shown in Fig. 9(a) and 9(b).

5.3 Twenty Five Level Cascaded H-Bridge Multilevel Inverter

The percentage total harmonic distortion analysis of the twenty five level diode clamped multilevel inverter is shown in Fig. 10(a) and cascaded H-bridge inverter shown in Fig. 10(b). The total harmonic distortion of both the multilevel inverter is almost same. The harmonic distortion of the diode clamped inverter is 2.81% and for cascaded H-bridge inverter is 2.82%. The total harmonic distortion for lower voltage levels in cascaded H-bridge inverter is better as compared to diode clamped multilevel inverter but for higher voltage levels the harmonic distortion is same for the both diode clamped and cascaded H-bridge multilevel inverter.

The variation of total harmonic distortion with different modulation index is given in Table 4, for diode clamped & cascaded H-bridge inverter. From the Table 4, it is observed that with increase in modulation index, the %THD is reduced for both types of inverters. The total harmonic distortion for both twenty five level multilevel inverters is almost same. But comparing the results with modulation control strategy the PD-PWM method gives better total harmonic distortion as compared with to the other methods.

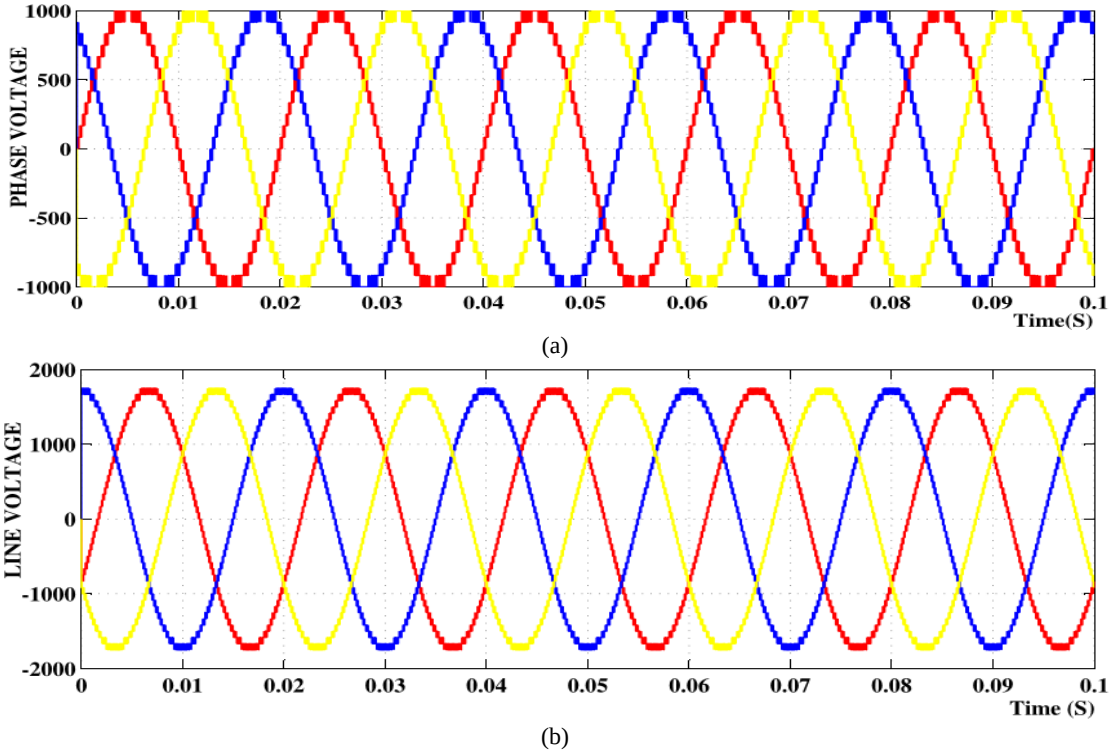
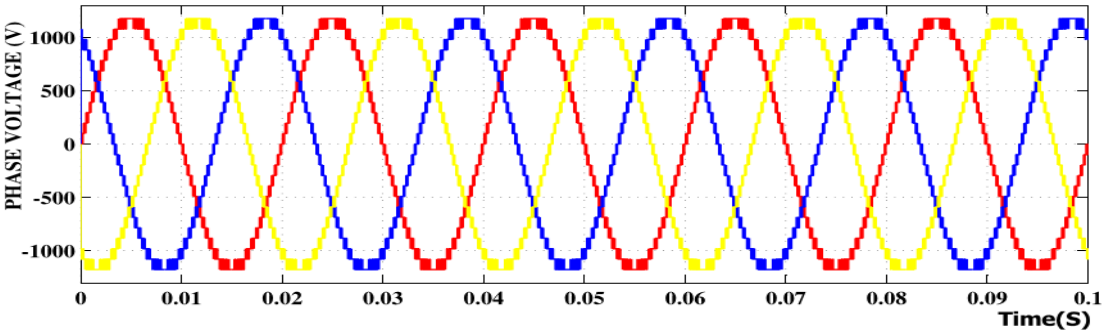
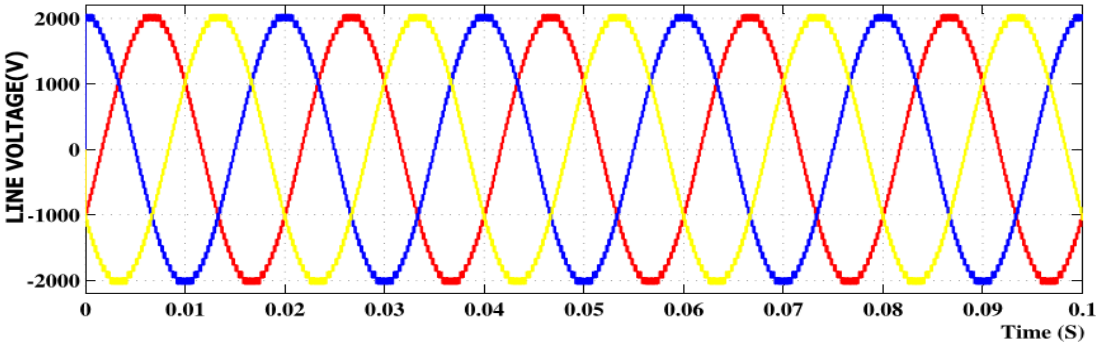


Fig. 8 Three phase output voltage of twenty five level diode clamped multilevel inverter a) phase voltage and b) line voltage.

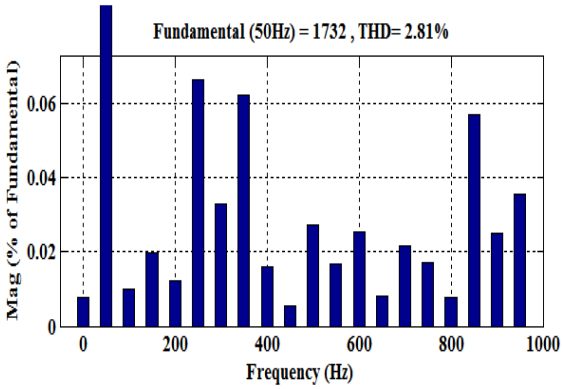


(a)

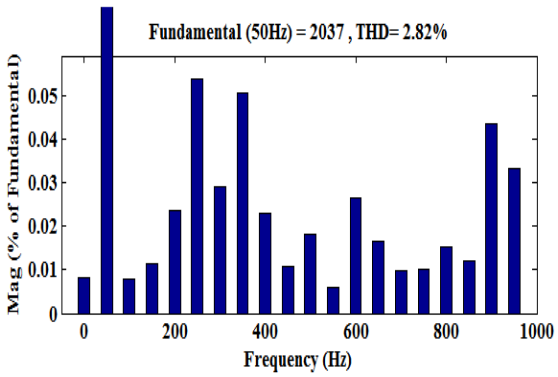


(b)

Fig. 9 Three phase output voltage of twenty five level cascaded H-bridge multilevel inverter a) phase voltage and b) line voltage.



(a)



(b)

Fig. 10 THD analysis of twenty five level inverter a) diode clamped and b) cascaded H-bridge.

Table 4 Variation of modulation index and its % total harmonic distortion of diode clamped & cascaded H-bridge inverter With PD, POD and APOD PWM control methods.

.Modulation Index	Diode clamped multilevel inverter THD (%)			Cascaded H-bridge multilevel inverter THD (%)		
	Modulation Control Strategy			Modulation Control Strategy		
	PD-PWM	POD-PWM	APOD-PWM	PD-PWM	POD-PWM	APOD-PWM
0.25	11.13	14.26	14.25	10.48	14.38	14.26
0.5	5.69	7.68	7.29	5.49	7.63	7.20
0.75	3.87	5.09	4.91	3.77	5.07	4.92
1.0	2.81	3.94	3.94	2.82	3.85	3.87

6 Conclusions

In this paper three phase twenty five level diode clamped and cascaded H-bridge inverter circuits using PD, POD and APOD PWM control methods are simulated and their output results are compared. From the results it has been observed that twenty five level cascaded H-bridge multilevel inverter output voltage is better as compared to twenty five level diode clamped multilevel inverter. But the total harmonic distortion of the both the inverter at higher levels almost same and both the inverters reduce the lower order harmonic largely by using fundamental switching. The PD-PWM

method has given better results as compared to other two PWM methods. From the output results it has been observed that by increasing number of levels in multilevel inverters the total harmonic distortion has reduced and its output voltage increased. Hence the filters requirement is avoided. In cascaded H-bridge multilevel inverter the number of components requirement is low as compared to diode clamped, so that cost and size of the system also reduced.

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